

6A Load Switch with Slew Rate Control and Discharge

Description

The AM6U2918 is a 7m Ω , 6A single-channel load switch that switches 0.9V to 5.5V power rails. It contains two overcurrent protection modes and configurable slew rate control. The product is packaged in a small 2.0x1.5mm package.

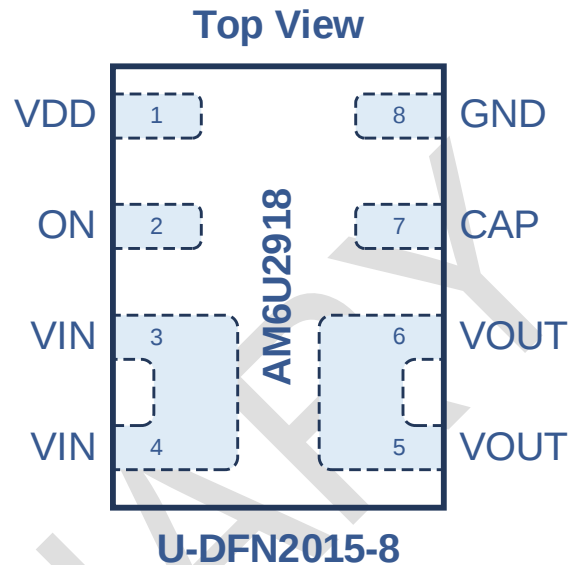
Features

- 2.0x1.5x0.55mm U-DFN2015-8 package
- 7m Ω typical RDS_{ON}
- Nominally supports up to I_{OUT} = 6A
- 150 Ω discharge resistor
- Two Over Current Protection Modes
 - Short Circuit Current Limit
 - Active Current Limit
- Over Temperature Protection
- RoHS Compliant / Halogen-Free / Pb-Free
- Operating Temperature: -40°C to 85°C
- Operating Voltage: 2.5V to 5.5V

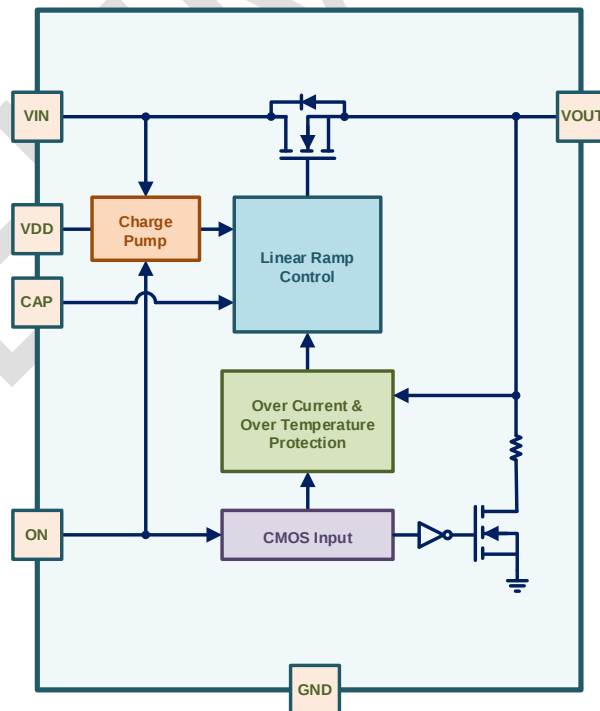
Applications

- Smartphones
- Tablets
- Notebooks

PIN Configuration



Functional Block Diagram



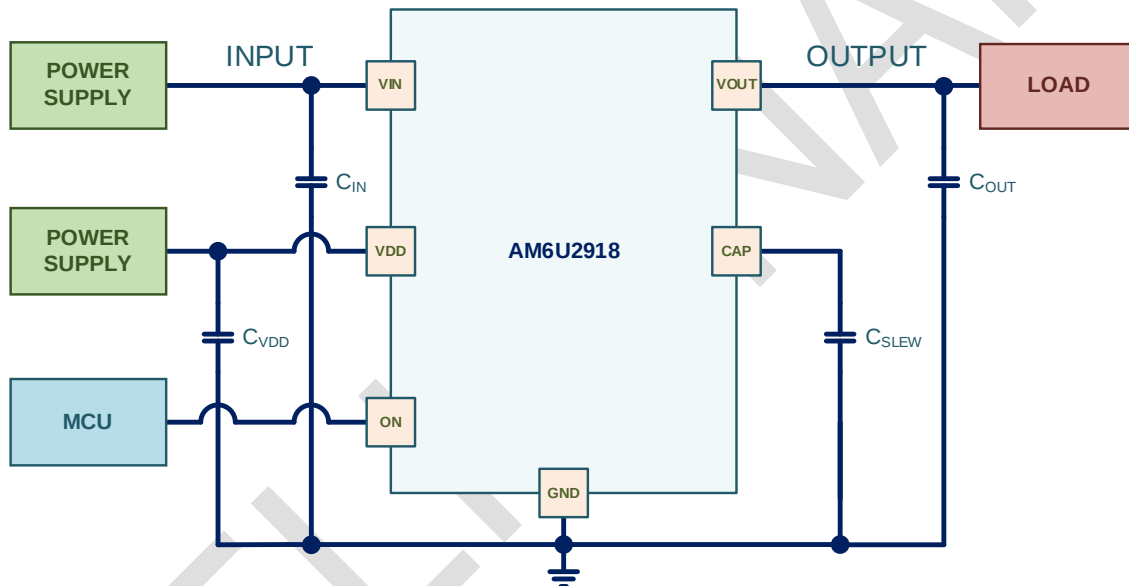


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Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	Power supply. Assumes a 0.1 μ F or larger decoupling capacitor.
2	ON	Input	Turns on load switch, active HI. There is an internal pull-down circuit to GND (~5 M Ω).
3 – 4	VIN	MOSFET	Drain terminal connection for the load switch. Connect at minimum a low-ESR 10 μ F capacitor from this pin to GND.
5 – 6	VOUT	MOSFET	Source terminal connection of the load switch. Connect a low-ESR capacitor from this pin to GND.
7	CAP	Input	Connects to a low-ESR ceramic capacitor to set the V _{OUT} slew rate.
8	GND	GND	Ground.

Typical Application Circuit





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Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply		—	—	7	V
T _S	Storage Temperature		-65	—	150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	—	—	V
MSL	Moisture Sensitivity Level		1			
W _{DIS}	Package Power Dissipation		—	—	1	W
MOSFET ID _{SPK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	—	—	6	A

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise stated. Typical values at T_A = 25°C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Recommended Operating Power Supply Voltage		2.5	—	5.5	V
V _{DDUVLO} ↓	VDD Undervoltage lock out falling		1.8	1.9	2.0	V
V _{DDUVLO_HYS}	VDD Undervoltage lock out hysteresis		—	0.1	—	V
V _{IN}	Recommended Operating Input Voltage		0.9	—	V _{DD}	V
V _{ON_VIH}	High Input Voltage on the ON pin		0.85	—	V _{DD}	V
V _{ON_VIL}	Low Input Voltage on the ON pin		-0.3	0	0.3	V
V _{ON_HYST}	ON pin Hysteresis		—	0.1	—	mV
I _{SHDN}	Input Shutdown Current	Disabled, I _{OUT} = 0A	—	—	100	nA
I _Q	Input Quiescent Current	Enabled, I _{OUT} = 0A	—	25	55	μA
I _{OUT}	Current from Drain to Source	Continuous	—	—	6	A
I _{LIMIT}	Active Current Limit	MOSFET will automatically limit current when V _{OUT} > 300mV	6.0	7.0	9.0	A
	Short Circuit Current Limit	MOSFET will automatically limit current when V _{OUT} < 300mV	—	0.5	—	
R _{DSon}	Switch On Resistance	T _A = 25°C; I _{OUT} = 100mA	—	7.3	8.5	mΩ
		T _A = 85°C; I _{OUT} = 100mA	—	8.5	10.0	
R _{Dis}	Discharge Resistance		100	150	200	Ω
R _{Pull_Down}	ON pull-down resistance		—	5	—	MΩ
t _{ON_Delay}	On Delay Time	50% ON to V _{OUT} Ramp Start	250	300	350	μs
t _{RISE}	Rise Time	10% V _{OUT} to 90% V _{OUT}	1.10	1.35	1.65	ms
		Example: C _{SLEW} = 3.9nF, V _{DD} = V _{IN} = 5V, C _{OUT} = 10μF, R _{LOAD} = 20Ω				
V _{OUT(SR)}	Slew Rate	10% V _S to 90% V _{OUT}	Configurable ²			V/ms
		Example: C _{SLEW} = 3.9nF, V _{DD} = V _{IN} = 5V, C _{OUT} = 10μF, R _{LOAD} = 20Ω	2.4	3.0	3.6	
t _{ON}	Total Turn On Time	50% ON to 90% V _{OUT}	Configurable ¹			ms
		Example: C _{SLEW} = 3.9nF, V _{DD} = V _{IN} = 5V, C _{OUT} = 10μF, R _{LOAD} = 20Ω	1.6	1.8	2.4	



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t _{OFF_Delay}	Off Delay Time	50% ON to V _{OUT} Fall Start, V _{DD} = V _{IN} = 5V; R _{LOAD} = 20Ω, no C _{OUT}	5	8	10	μs
t _{FALL}	Fall Time	90% V _{OUT} to 10% V _{OUT} V _{DD} = V _{IN} = 5V; R _{LOAD} = 20Ω, no C _{OUT}	4	5	6	μs
t _{OFF}	Total Turn Off Time	50% ON to 10% V _{OUT} V _{DD} = V _{IN} = 5V; R _{LOAD} = 20Ω, no C _{OUT}	9	13	16	μs
C _{OUT}	Output Load Capacitance	C _{OUT} connected from V _{OUT} to GND	—	10	500	μF
OTP	Overtemperature Protection	Threshold	—	125	—	°C
		Hysteresis	—	25	—	°C
Notes:						
1. Refer to typical timing parameter vs. C _{SLEW} performance charts for additional information.						



Typical Performance Characteristics

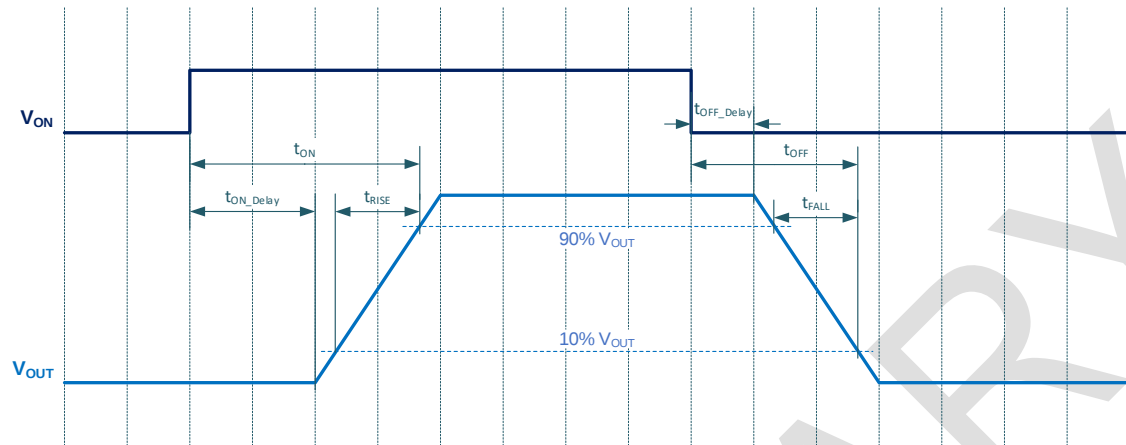


Figure 1. Basic timing parameters.



Application Information

Typical Operation

For correct operability per the AM6U2918 EC table a proper power-up sequence must be applied. Apply V_{DD} first, followed by V_{IN} , then ON signal to power-up the device. In order to control the inrush current from capacitive loads, set a desired linear output slew rate by placing a corresponding C_{SLEW} capacitor between CAP pin and GND. The greater the capacitor value at CAP pin, the slower the output ramp.

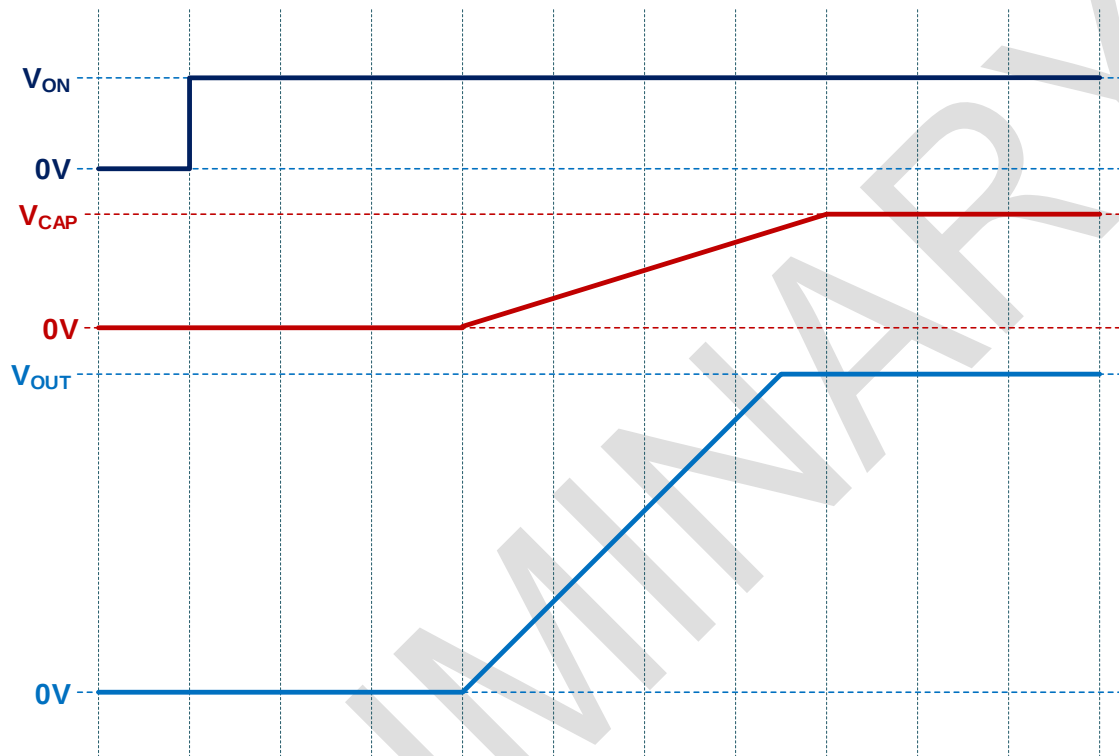
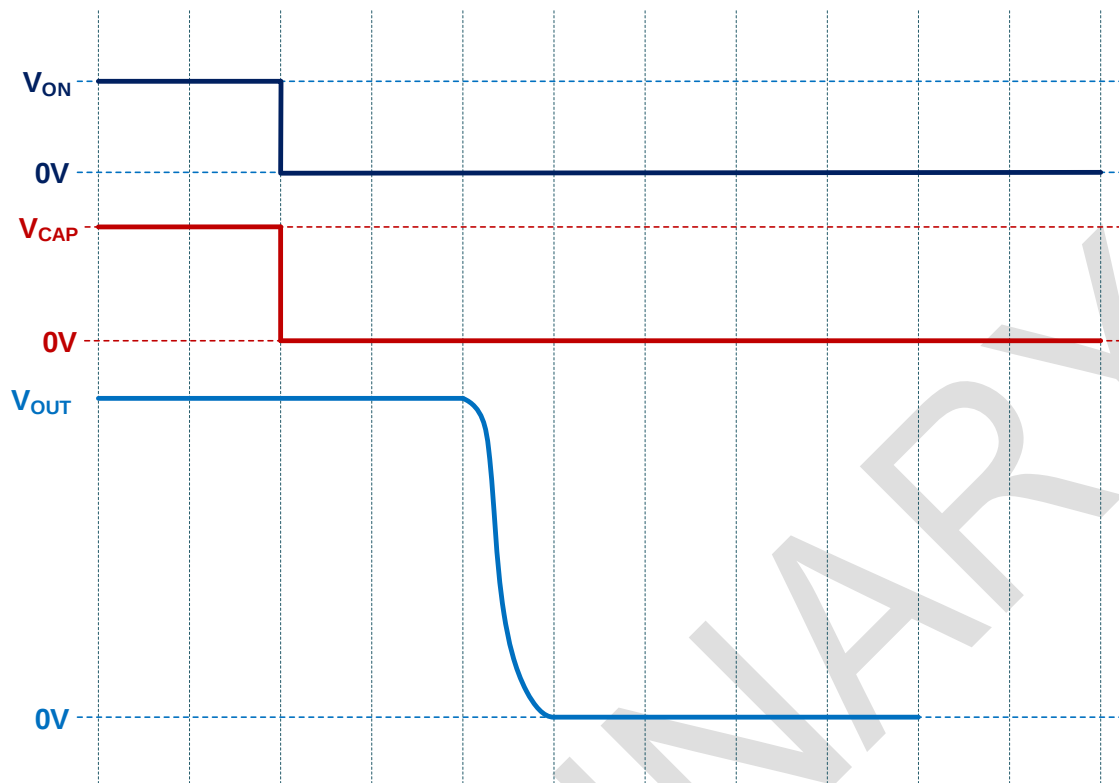
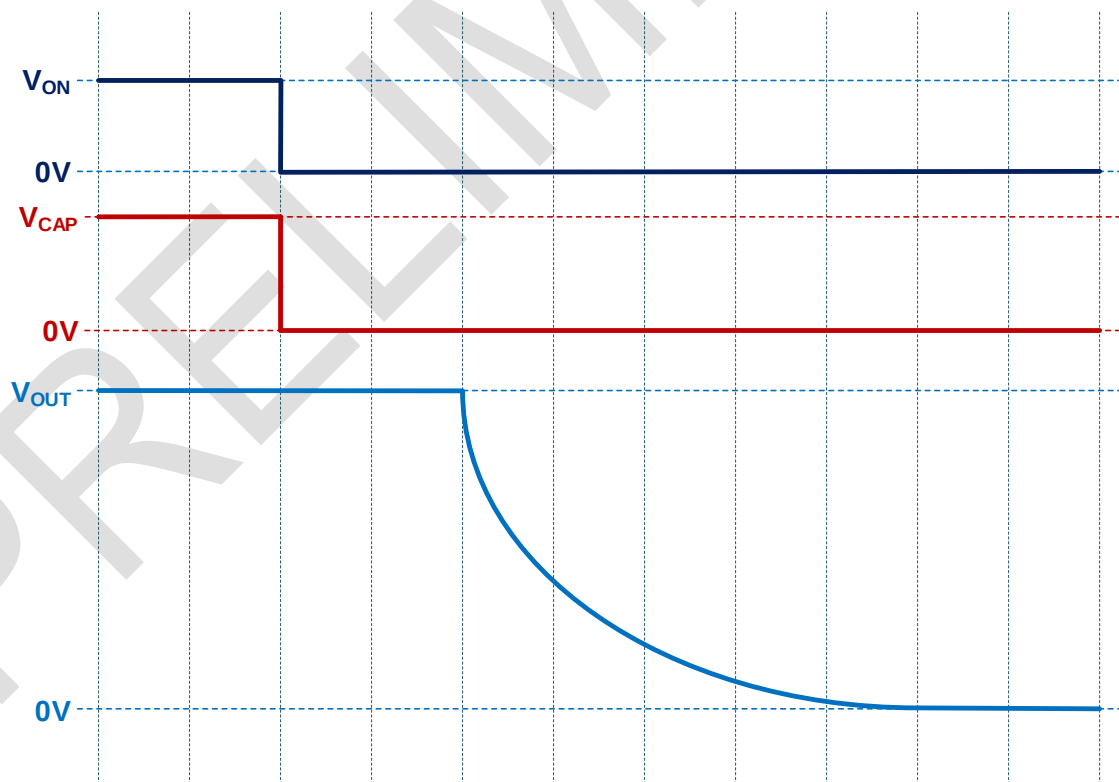


Figure 2. AM6U2918 typical power-up operation.



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Figure 3. AM6U2918 typical power-down operation. No C_{OUT} condition.Figure 4. AM6U2918 typical power-down operation. C_{OUT} condition.



Overtemperature Protection

The AM6U2918 contains an overtemperature protection feature, which is primary protection for the part. If the internal junction temperature of the AM6U2918 reaches 125°C, such as during an overcurrent event, the FET is shut off completely so the die can cool. Once the die temperature reaches approximately 100°C Overtemperature Protection will disable and the FET will again be capable of conducting. This event will repeat for as long as the condition exists which causes the die to overheat.

When OTP event occurs, the part resets including Ramp Control Circuit in order to have a controlled power up on the next iteration after the die cools down. Depending on the load conditions V_{OUT} should not necessarily be discharged completely.

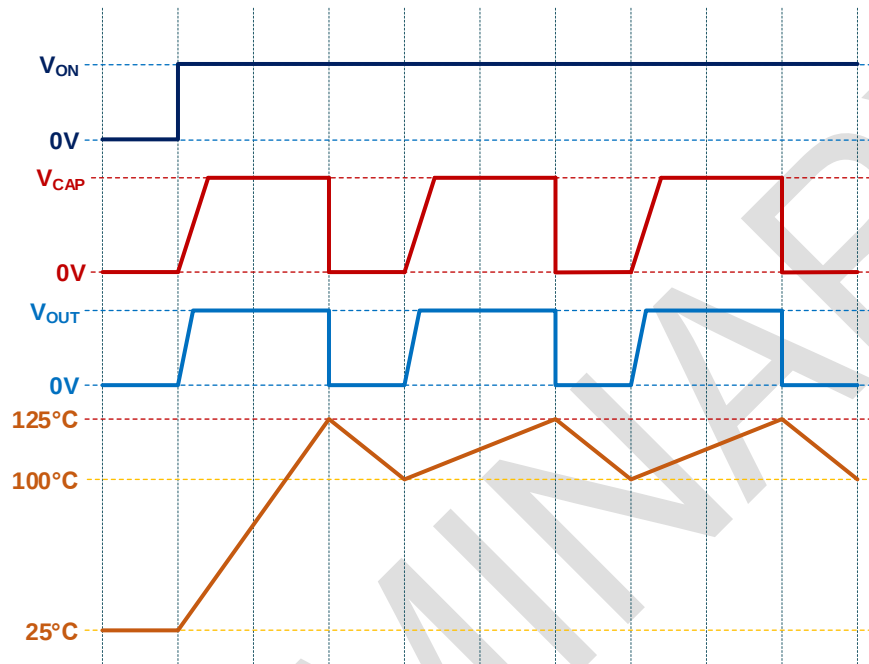


Figure 5. AM6U2918 typical overtemperature protection operation.



Current Limiting Operation

The AM6U2918 has two types of current limiting triggered by the VOUT pin voltage:

- Active Current Limit (ACL): $V_{OUT} > 300\text{mV} - 7\text{A}$.
- Short Circuit Current Limit (SCL): $V_{OUT} < 300\text{mV} - 500\text{mA}$.

The current is limited with output voltage by increasing the $R_{DS(on)}$ value. If an overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed OTP Threshold specification, the FET is shut Off completely to allow the die to cool. When the die cools by the listed OTP Hysteresis temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

Active Current Limit Mode

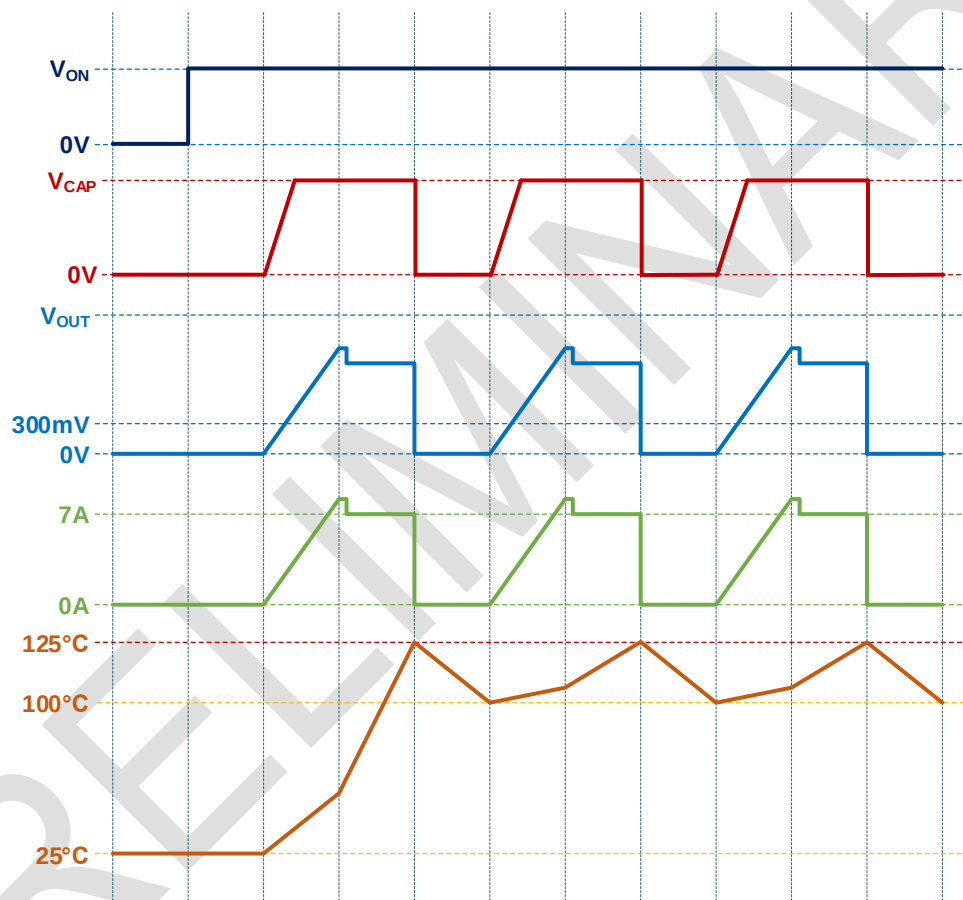


Figure 6. AM6U2918 ACL+OTP operation during power up on overload condition.



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Short Circuit Current Limit Mode

The AM6U2918 also contains a short circuit limit, which will trigger in the event that V_{OUT} is externally limited to 300mV or less. During this event, the AM6U2918 will maintain the resistivity of the FET so as to limit the output current of the device to a typical value of 500mA. If the Short-circuit event is resolved the AM6U2918 will continue its voltage ramp per the slew rate set by the capacitor on the CAP pin.

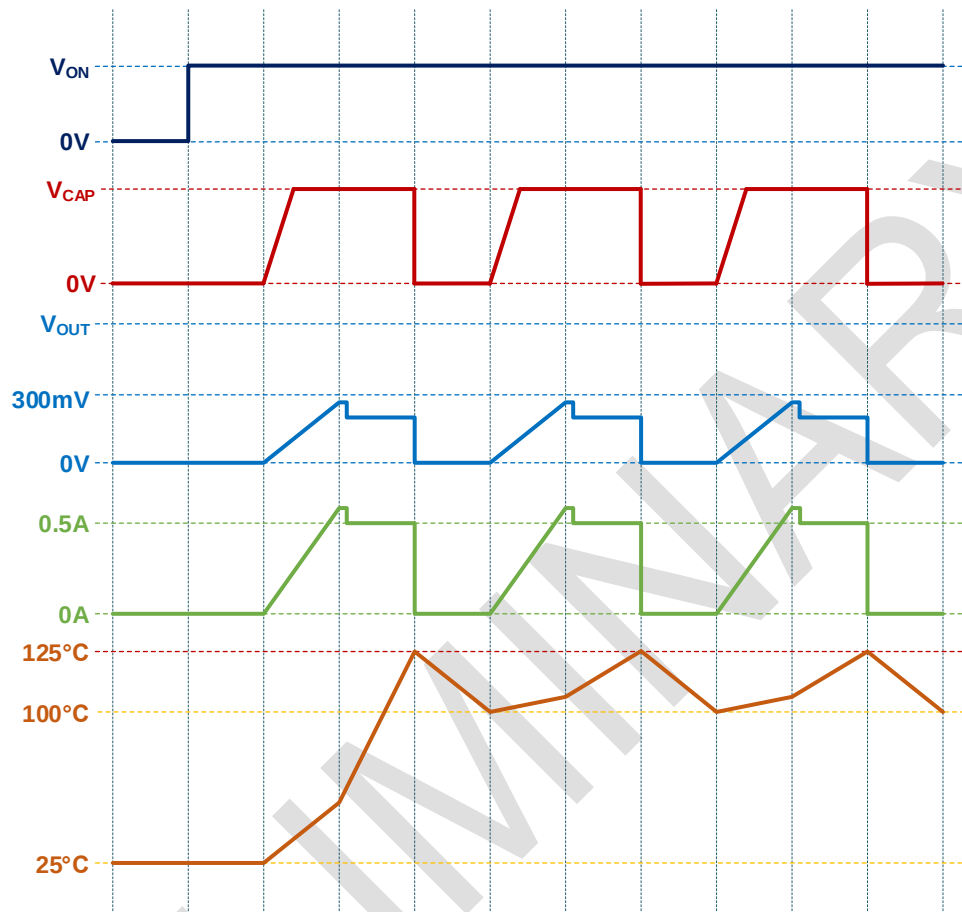


Figure 7. AM6U2918 SCL+OTP operation.

Note: Depending upon factors such as V_{IN} , the shorted value of V_{OUT} , and ambient temperature, the AM6U2918 may or may not dissipate enough power to trigger the Overtemperature Protection within the circuit. If the overtemperature protection occurs the part will shut down and retry per the Overtemperature Detection description above.



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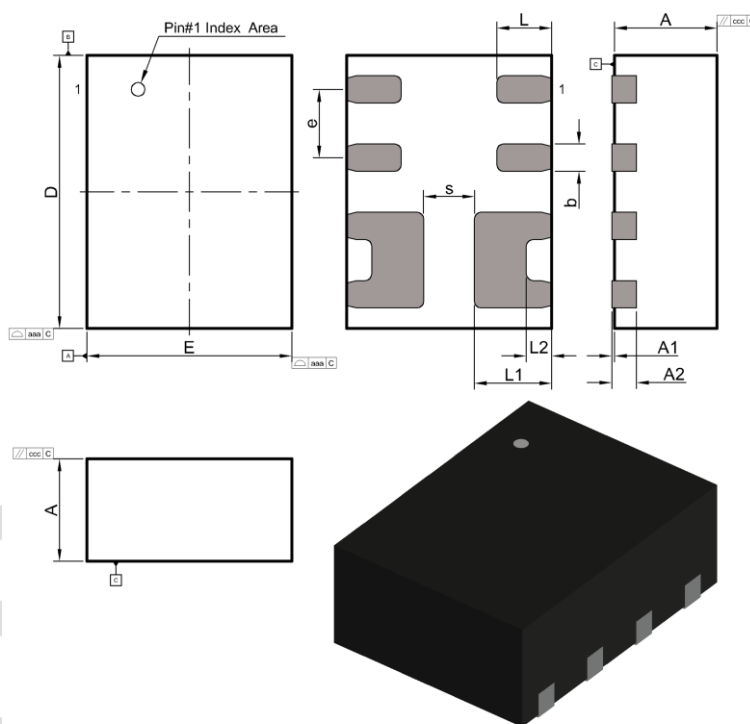
Package Top Marking



NN – Identification Code: DV
Y – Year: 0~9
W – Week: A~Z – 1~26 week
a~z – 27~52 week, z represents 52 and 53 week
N – Internal Code

Package Outline Dimensions

U-DFN2015-8

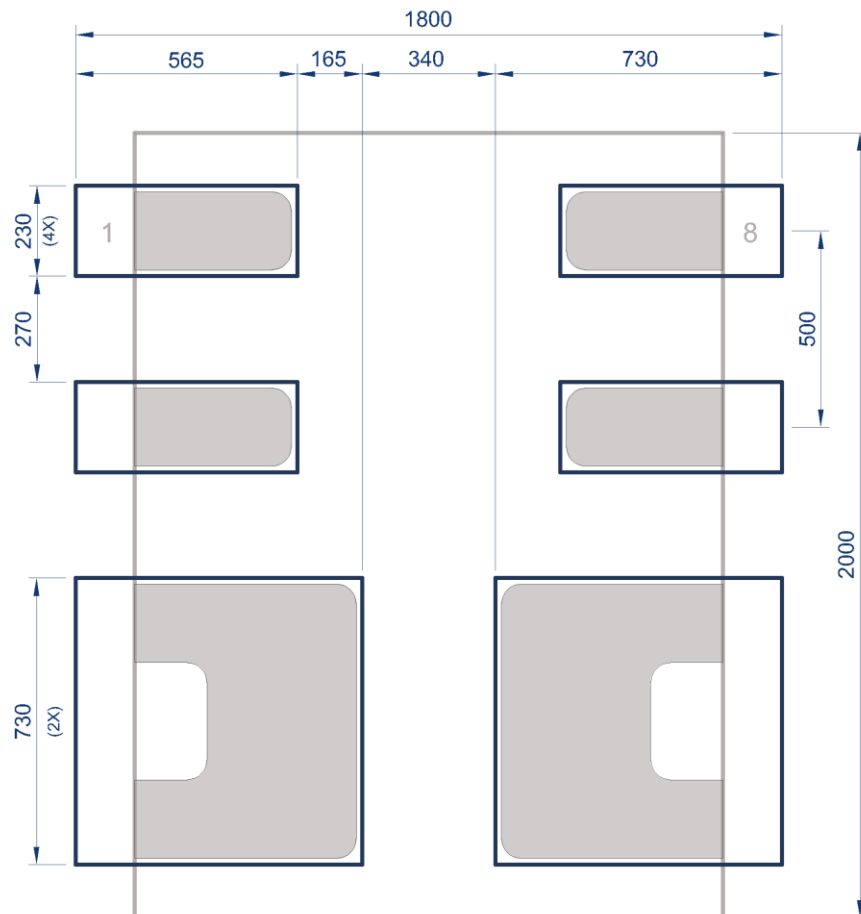


Symbol	Min.	Typ.	Max.	Symbol	Min.	Typ.	Max.
A	0.500	0.550	0.600	L	0.375	0.400	0.425
A1	-0.005	—	0.030	L1	0.515	0.565	0.615
A2	0.225	0.250	0.275	L2	0.135	0.185	0.235
b	0.175	0.200	0.225	s	—	0.370	—
D	1.950	2.000	2.050	aaa	—	0.050	—
E	1.450	1.500	1.550	ccc	—	0.050	—
e	—	0.500	—				
All Dimensions in mm							



Suggested Pad Layout

U-DFN2015-8





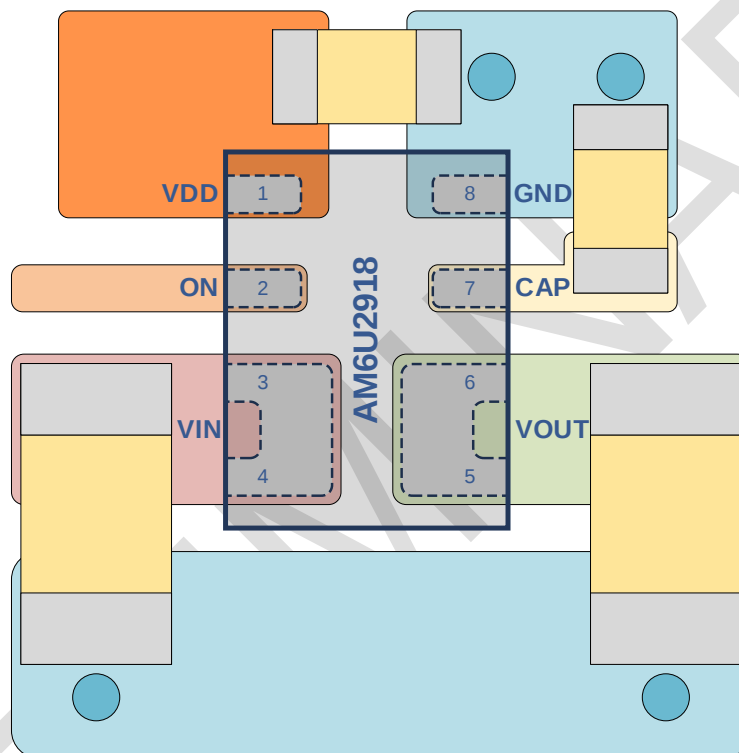
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Recommended Layout

It is important to have a proper PCB layout for high-performance device operation. The list below provides some basic rules for PCB layout.

- Connect a 0.1 μ F capacitor from VDD pin to GND. It should be placed as close to the device as possible.
- Place high-quality low-ESR input C_{IN} (10 μ F min) and output C_{OUT} capacitors close to the device Drain and Source pins to minimize the effects of parasitic inductance.
- Make sure to have a solid Ground connection.
- All traces should be as short, wide and direct as possible.
- Drain and Source pins have the most heat dissipation during high-current operations. Use polygon planes and/or 2 oz. copper for Drain and Source connections.

The example below illustrates described layout guidelines implementation.



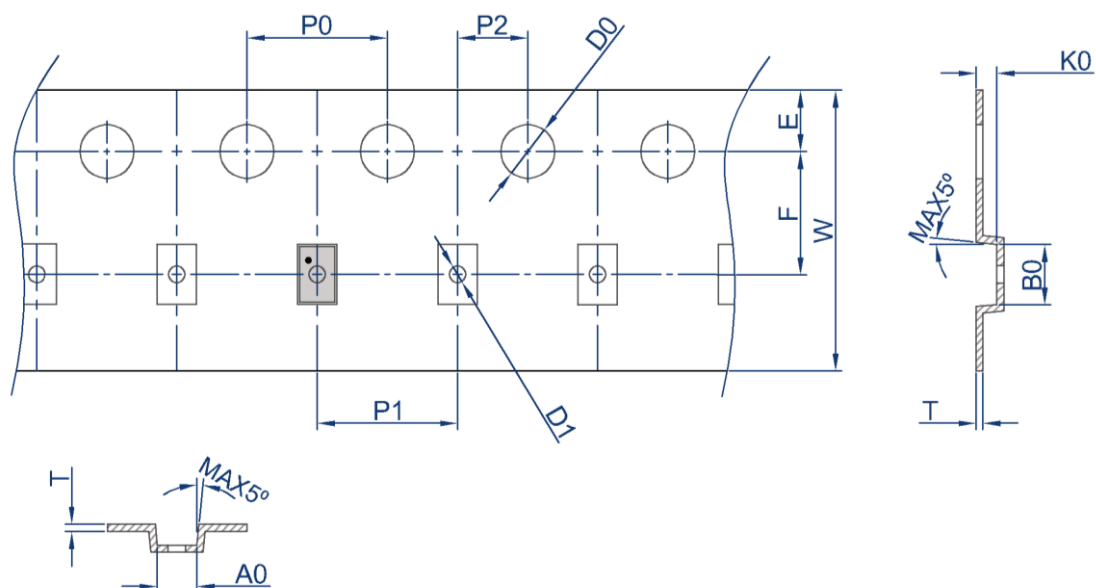


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Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
U-DFN2015-8	8	1.5x2.0x0.55	3,000	3,000	178/60	100	400	100	400	8	4

Package Type	A0	B0	K0	P0	P1	P2	T	D0	D1	E	F	W
U-DFN2015-8	1.68	2.18	0.7	4	4	2	0.2	1.55	0.50	1.75	3.5	8





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Revision History

Date	Version	Change
October 24, 2024	Rev.001	Initial release

PRELIMINARY



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