AM6U1104

4A Load Switch with Slew Rate Control and Discharge

Description

The AM6U1104 is a 4mΩ, 4A single-channel load switch that switches 0.9V to 5.5V power rails. It contains two overcurrent protection modes, configurable slew rate control and output discharge features.

The product is packaged in small 1.6x2.5mm package.

Features

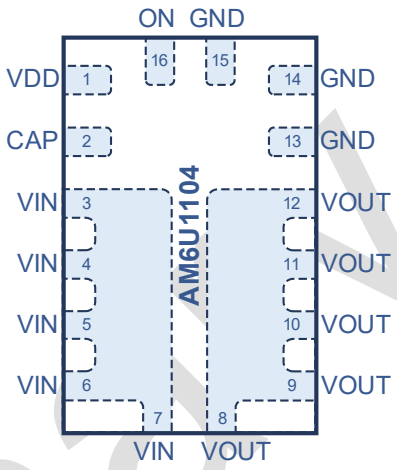
- 1.6x2.5x0.55mm QFN1625-16 package
- 4mΩ RDS_{ON}
- Discharges load when off
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- RoHS Compliant / Halogen-Free / Pb-Free
- Operating Temperature: -40°C to 85°C
- Operating Voltage: 2.5V to 5.5V

Applications

- Smartphones
- Tablets
- Notebooks

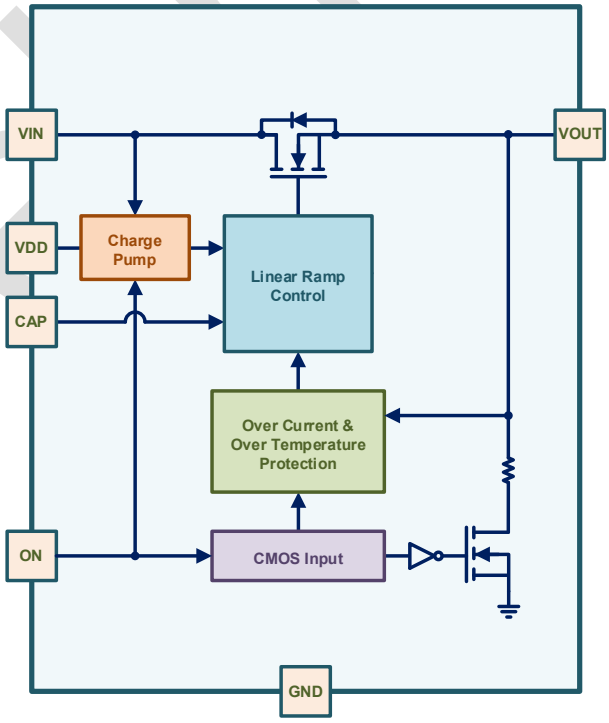
PIN Configuration

Top View



U-QFN1625-16

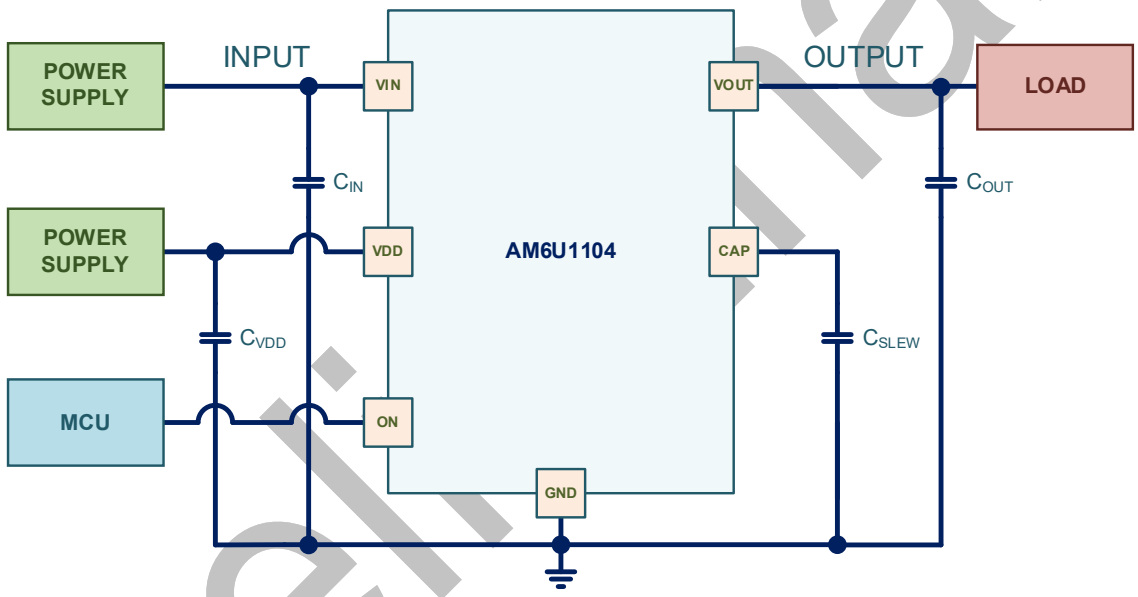
Functional Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	Power supply. Assumes a 0.1µF or larger decoupling capacitor.
2	CAP	Input	Connects to a low-ESR ceramic capacitor to set the V_{OUT} slew rate.
3 – 7	VIN	MOSFET	Drain terminal connection for the load switch. Connect at minimum a low-ESR 10µF capacitor from this pin to GND.
8 – 12	VOUT	MOSFET	Source terminal connection of the load switch. Connect a low-ESR capacitor from this pin to GND.
13 – 15	GND	GND	Ground.
16	ON	Input	Turns on load switch, active HI. There is an internal pull-down circuit to GND (~5MΩ).

Typical Application Circuit



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		—	—	6	V
T_S	Storage Temperature		-65	—	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	—	—	V
MSL	Moisture Sensitivity Level			1		
W_{DIS}	Package Power Dissipation		—	—	1.2	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1ms with 1% duty cycle	—	—	6	A

Electrical Characteristics

T_A = -40 °C to 85 °C unless otherwise stated. Typical values at T_A = 25 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		2.5	—	5.5	V
$V_{DD(UVLO)}$	V_{DD} Undervoltage Lockout Threshold	V_{DD} ↑	1.6	1.9	2.2	V
		V_{DD} ↓	1.5	1.8	2.1	
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0A		—	60	nA
I_Q	Input Quiescent Current	Enabled, I_{OUT} = 0A	—	25	55	µA
I_{FET_OFF}	MOSFET OFF Leakage Current	2.5V ≤ V_{DD} ≤ 5.5V; V_{OUT} = 0V, ON = LOW, T_A = 25°C	—	—	1	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A = 25°C; I_{OUT} = 100mA	—	4.2	5.2	mΩ
		T_A = 85°C; I_{OUT} = 100mA	—	5.2	6.3	
I_{OUT}	Current from Drain to Source	Continuous	—	—	4	A
V_{IN}	Input Voltage		0.9	—	V_{DD}	V
t_{ON_Delay}	ON Delay Time	50% ON to V_{OUT} Ramp Start	—	300	500	µs
t_{ON}	Total Turn On Time	50% ON to 90% V_{OUT}		Configurable [1]		ms
		Example: C_{SLEW} = 3.9nF, V_{DD} = V_{IN} = 5V, C_{OUT} = 10µF, R_{LOAD} = 20Ω	—	1.7	—	
		Example: C_{SLEW} = 10nF, V_{DD} = 5V, V_{IN} = 1.8V, C_{OUT} = 500µF, R_{LOAD} = 50Ω	—	1.6	—	
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT}		Configurable [1]		V/ms
		Example: C_{SLEW}= 3.9nF, V_{DD} = V_{IN} = 5V, C_{OUT} = 10µF, R_{LOAD} = 20Ω		2.9		
C_{OUT}	Output Load Capacitance	C_{OUT} connected from VOUT to GND	—	10	600	µF
R_{DIS}	Discharge resistance		0.8	1.1	1.4	Ω
V_{IH}	ON Pin High Input Voltage		0.85	—	V_{DD}	V
V_{IL}	ON Pin Low Input Voltage		-0.3	0	0.3	V
I_{LIMIT}	Active Current Limit	MOSFET will automatically limit current when V_{OUT} > 300mV	5.5	7.0	9.0	A

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
	Short Circuit Current Limit	MOSFET will automatically limit current when V_{OUT} < 300mV	—	1.0	—	
$THERM_{ON}$	Thermal shutoff turn-on temperature		—	150	—	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		—	130	—	°C
$THERM_{TIME}$	Thermal shutoff time		—	—	1	ms
t_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start, V_{DD} = V_{IN} = 5V; R_{LOAD} = 20Ω, no C_{OUT}	—	6.5	—	μs
R_{Pull_Down}	ON pull-down resistance	V_{DD} = V_{IN} = 5V	—	4.6	—	MΩ

Notes:

1. Compliance to the datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information.

Typical Performance Characteristics

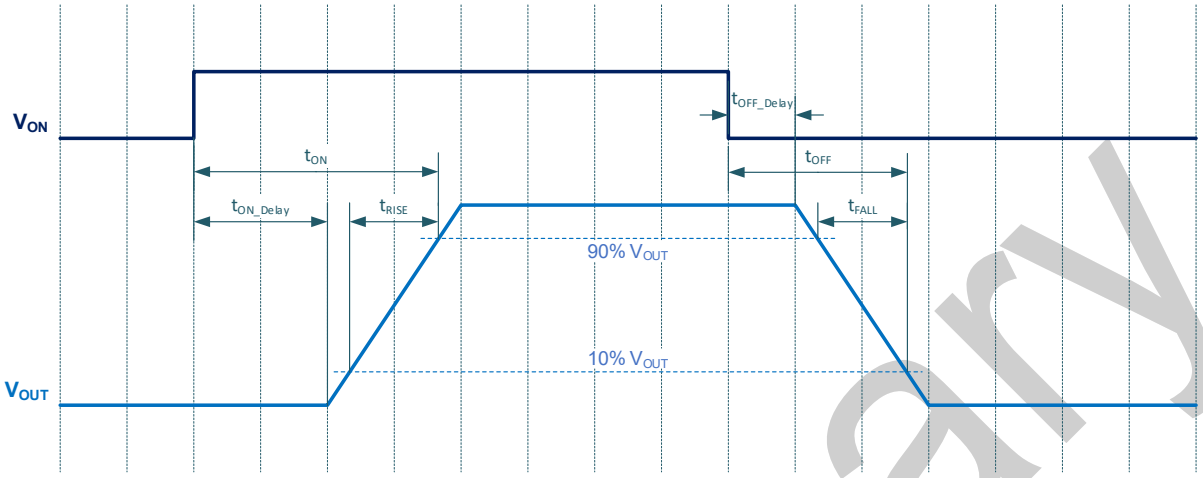


Figure 1. Basic Timing Parameters

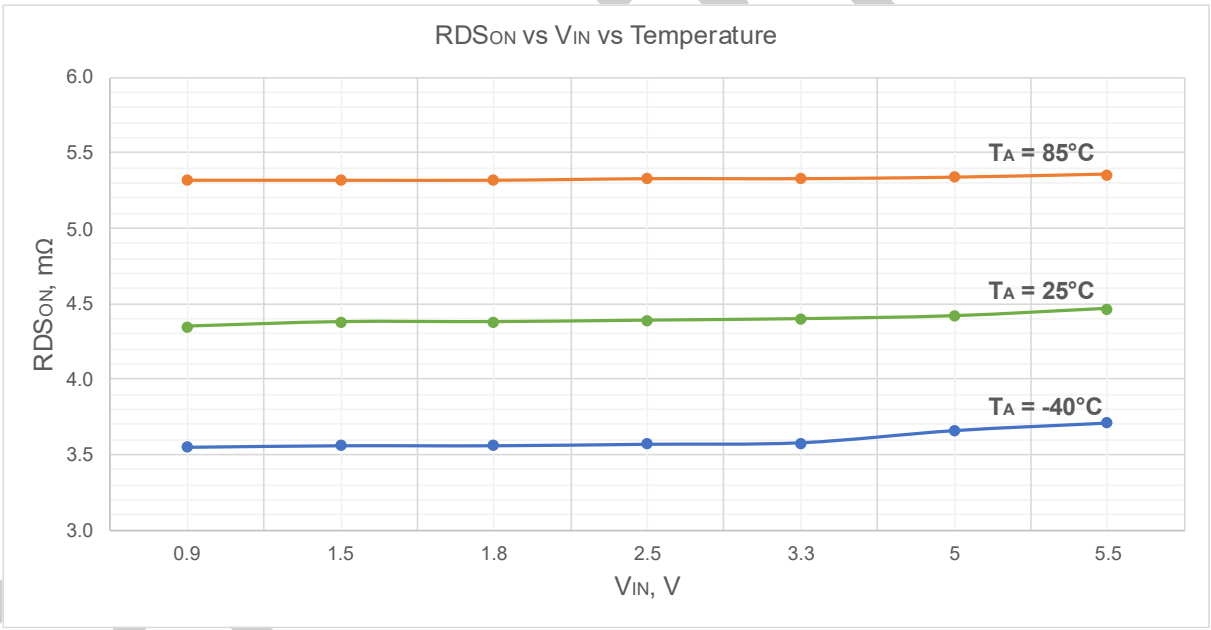


Figure 2. RDS_{ON} vs. V_{IN} and Temperature at V_{DD} = 5.5V and I_{OUT} = 100mA.

Application Information

Typical Operation

For correct operability per the AM6U1104 EC table a proper power-up sequence must be applied. Apply V_{DD} first, followed by V_{IN}, then ON signal to power-up the device. In order to control the inrush current from capacitive loads, set a desired linear output slew rate by placing a corresponding C_{SLEW} capacitor between CAP pin and GND. The greater capacitor value at CAP pin, the slower the output ramp.

During operation, should a system fault occur, V_{IN} should be returned to Recommended Operating Conditions before the load switch is transitioned between its on and off states to reduce out-of-spec transitional stress on the device.

Some typical operation waveforms are illustrated below.

Figure 3. AM6U1104 Typical Power-Up Operation Waveform. VDD = V_{IN} = 5V, R_{LOAD} = 20Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF

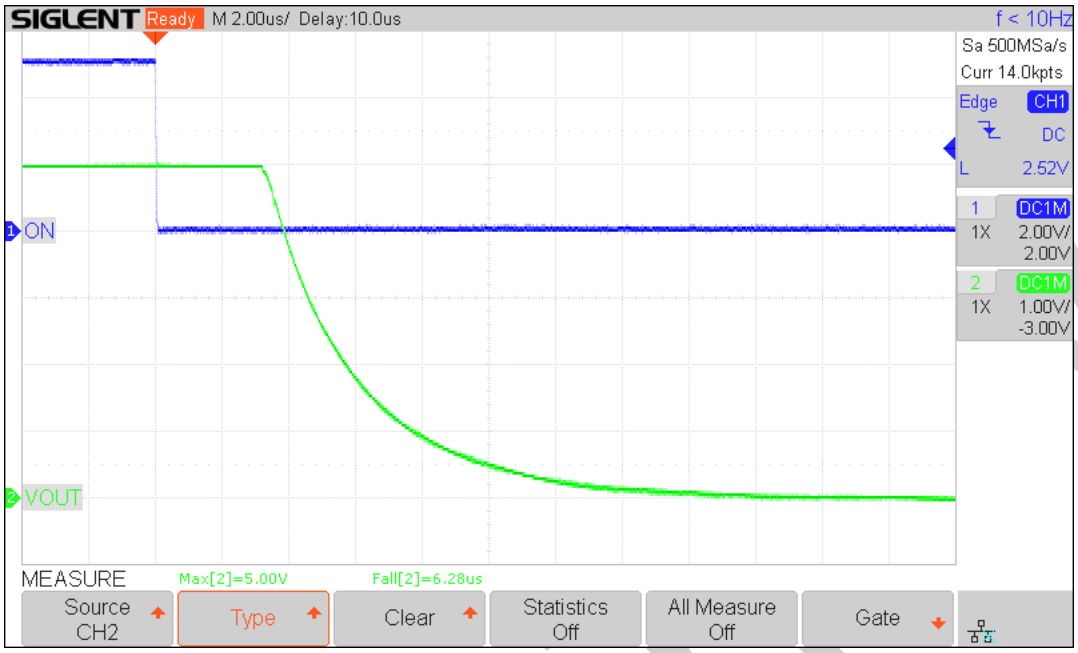


Figure 4. AM6U1104 Typical Power-Down Operation Waveform. V_{DD} = V_{IN} = 5V, R_{LOAD} = 20Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF

Overtemperature Protection

The AM6U1104 contains an overtemperature protection feature. If the internal junction temperature of the AM6U1104 reaches 150°C, such as during an overcurrent event, the FET is shut off completely so the die can cool. Once the die temperature reaches approximately 130°C Overtemperature Protection will disable and the FET will again be capable of conducting. This event will repeat for as long as the condition exists which causes the die to overheat.

Current Limiting Operation

The AM6U1104 has two types of current limiting triggered by the output VOUT pin voltage.

1. Active Current Limiting Mode (with Thermal Shutdown Protection)

When voltage V_{OUT} > 300 mV the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the load switch's I_{ACL} threshold.

If a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the load switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely to allow the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

The AM6U1104 also contains a short circuit limit, which will trigger in the event that V_{OUT} is externally limited to 300mV or less due to an improper solder connection or similar defect on the same node as the VOUT pin. During this event, the AM6U1104 will maintain the resistivity of the FET so as to limit the output current of the device to a typical value of 1000mA.

If the Short-circuit event is resolved the AM6U1104 will continue its voltage ramp per the slew rate set by the capacitor on the CAP pin.

Note: Depending upon factors such as V_{IN}, the shorted value of V_{OUT}, and ambient temperature, the AM6U1104 may or may not dissipate enough power to trigger the Overtemperature Protection within the circuit. If the overtemperature protection occurs the part will shut down and retry per the Overtemperature Detection description above.

Package Outline Dimensions

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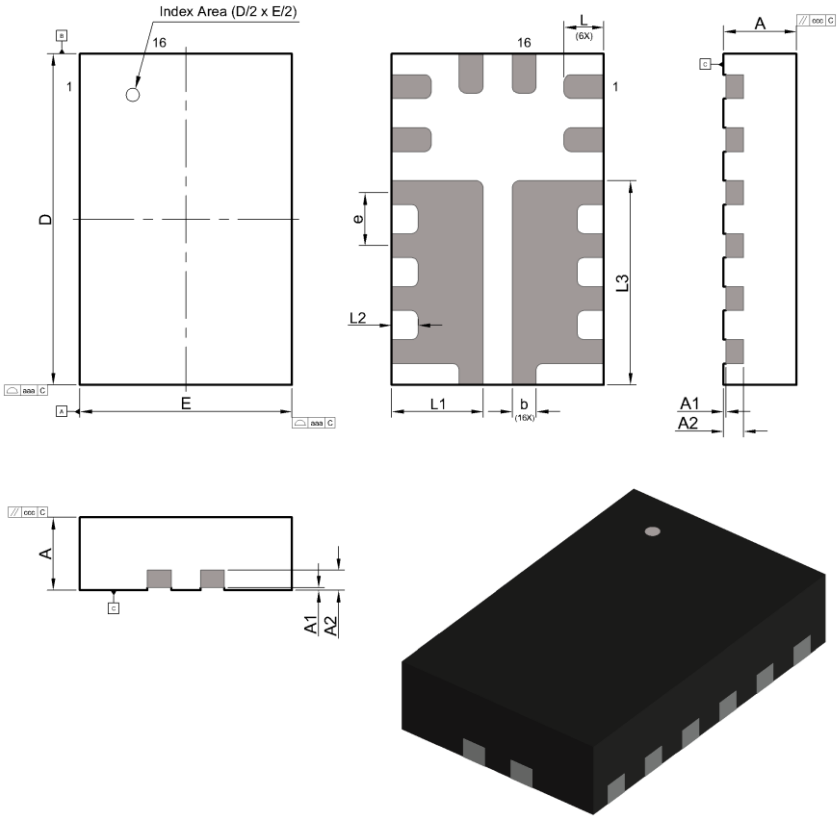


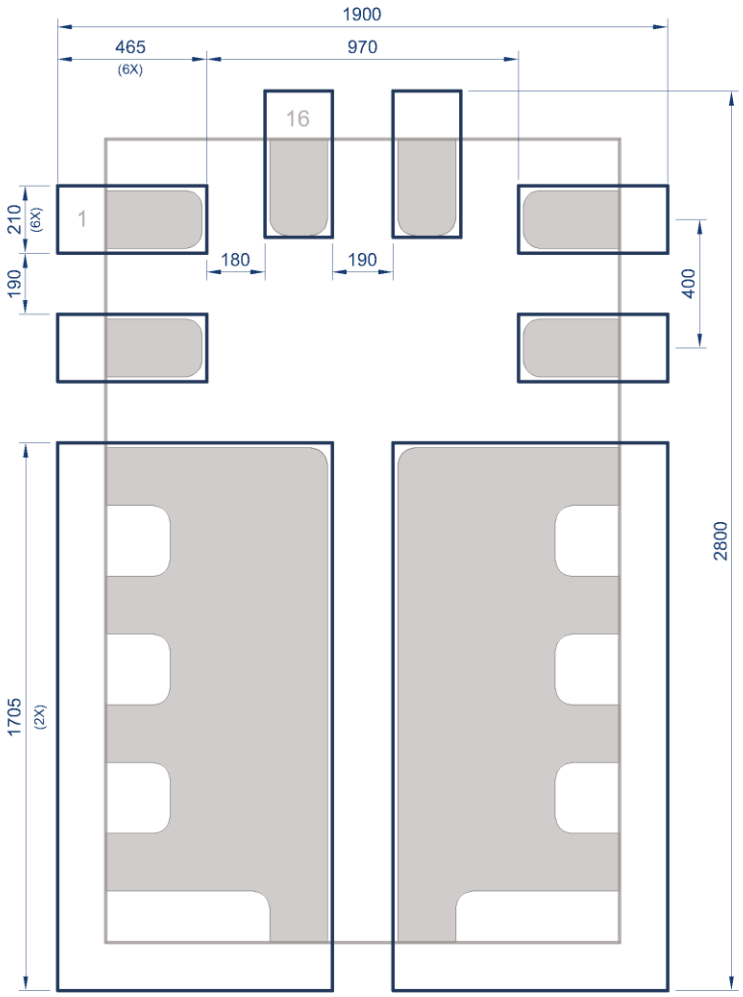
Symbol	Min.	Typ.	Max.	Symbol	Min.	Typ.	Max.
A	0.500	0.550	0.600	**L**	0.275	0.300	0.325
A1	0.010	—	0.000	**L1**	0.640	0.690	0.740
A2	0.125	0.150	0.175	**L2**	—	0.200	—
b	0.155	0.180	0.205	**L3**	1.490	1.540	1.590
D	2.450	2.500	2.550	**aaa**	—	0.050	—
E	1.550	1.600	1.650	**ccc**	—	0.050	—
e	—	0.400	—				
All Dimensions in mm							

Package Top Marking

NN – Identification Code: B2
Y – Year: 0~9
W – Week: A~Z – 1~26 week
a~z – 27~52 week, z represents 52 and 53 week
N – Internal Code

Suggested Pad Layout

U-QFN1625-16

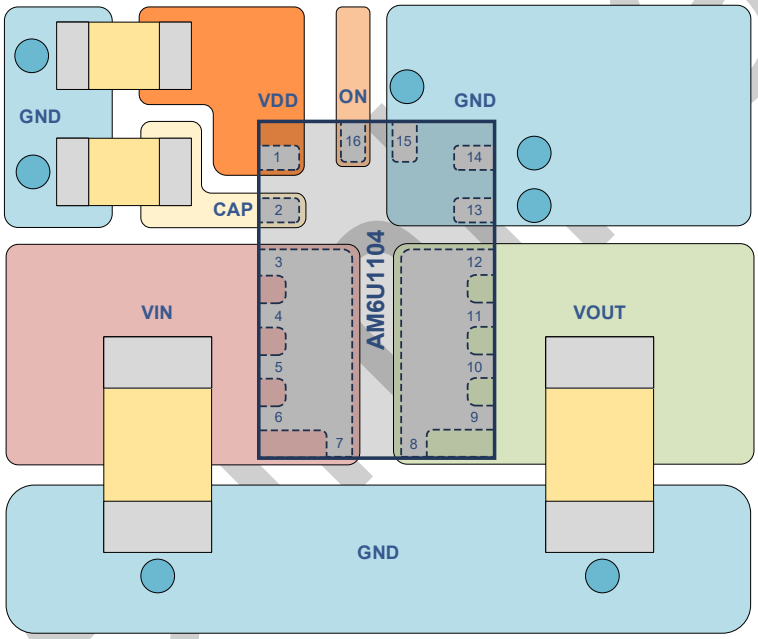


Recommended Layout

It is important to have a proper PCB layout for high-performance device operation. The list below provides some basic rules for PCB layout.

- Connect a 0.1µF capacitor from VDD pin to GND. It should be placed as close to the device as possible.
- Place high-quality low-ESR input C_{IN} (10µF min) and output C_{OUT} capacitors close to the device Drain and Source pins to minimize the effects of parasitic inductance.
- Make sure to have a solid Ground connection.
- All traces should be as short, wide and direct as possible.
- VIN and VOUT pins have the most heat dissipation during high-current operations. Use polygon planes and/or 2 oz. copper for VIN and VOUT connections.

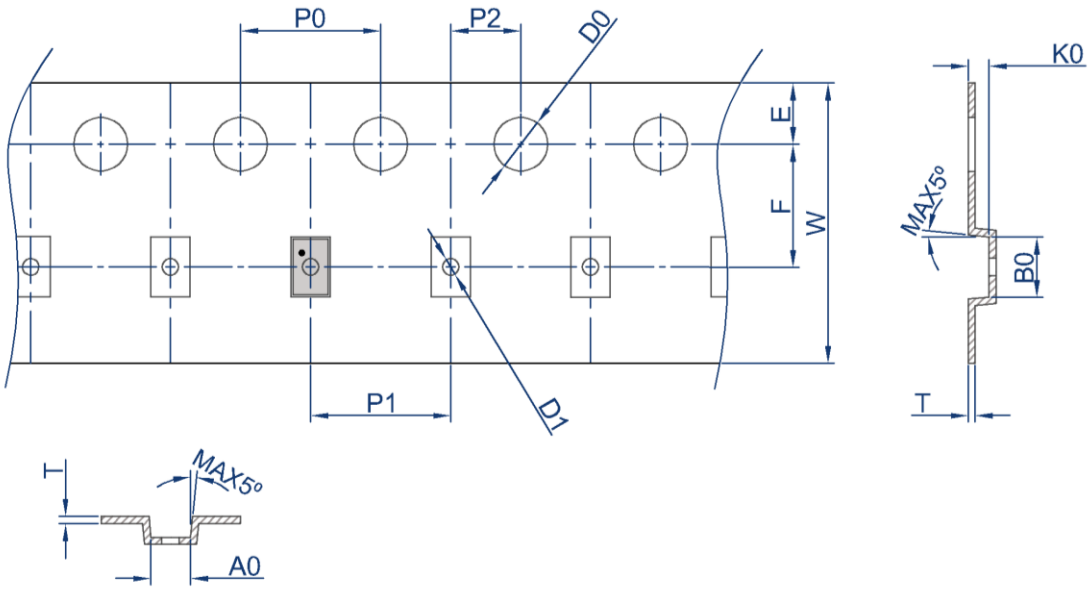
Example below illustrates described layout guidelines implementation.



Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
U-QFN1625-16	16	1.6 x2.5 x 0.55	3,000	3,000	178/60	100	400	100	400	8	4

Package Type	A0	B0	K0	P0	P1	P2	T	D0	D1	E	F	W
U-QFN1625-16	1.8	2.8	0.70	4.00	4.00	2.00	0.20	1.55	0.50	1.75	3.50	8.00



Revision History

Date	Version	Change
June 15,2023	Rev.001	Initial release
November 5, 2024	Rev.002	Updated pinout drawing. Corrected typos
June 5, 2025	Rev.003	Updated Recommended Layout. Added Laser Marking section

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