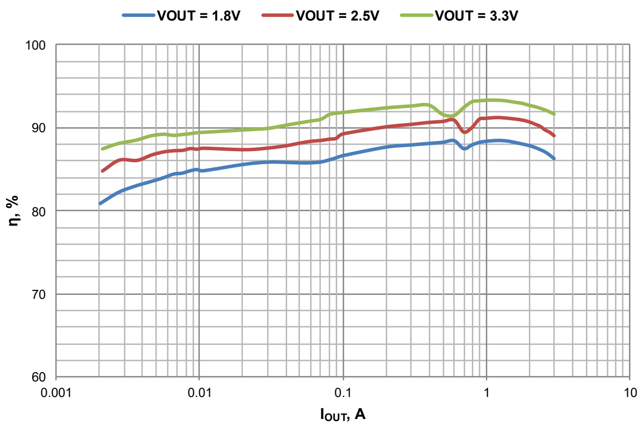
2.4V TO 5.5V INPUT, PROGRAMMABLE 3A BUCK CONVERTER

Description

The AM32103 is a programmable step-down converter with an input voltage range of 2.4V to 5.5V. The maximum output current is 3A, and the output voltage ranges from 0.6V to 3.8V. Key features include an ultra-low 16 µA quiescent current, selectable operating modes (Auto, FPWM, Sleep and USM), and a configurable switching frequency ranging from 2MHz to 3MHz. Integrated power transistors, precision regulation (±1%) in PWM, and protection functions (UVLO, OVP, SCP, thermal shutdown) make the AM32103 ideal for space-constrained and battery-powered systems.

Applications

- IoT devices
- Cell Phones
- Portable Devices
- Optical Modules



Efficiency vs Output Current,

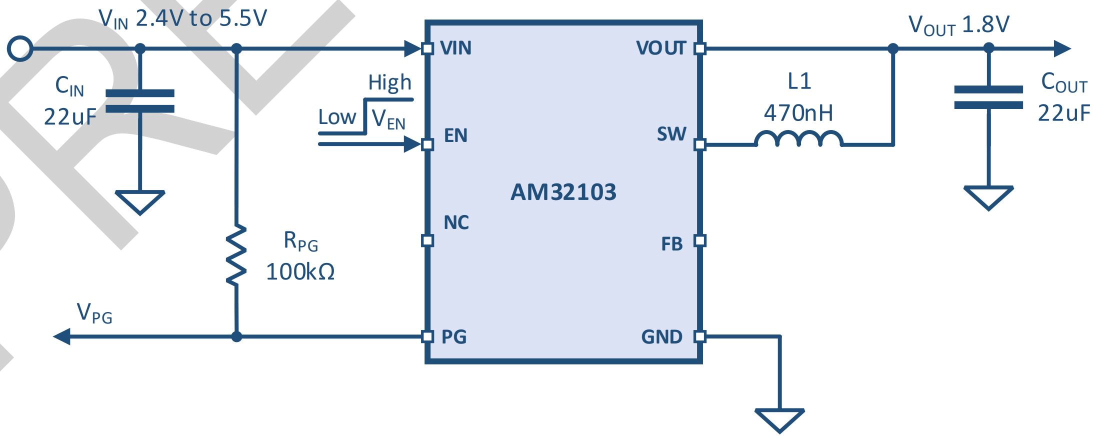
V_{IN}=5.0V, F_{SW}=2MHz, Mode=Auto, Internal Divider

Features

- 2.4V to 5.5V input voltage range
- Flexible Output Voltage Selection:
  - Internal voltage dividers: 0.6V, 0.9V, 1.1V, 1.8V, 2.5V, or 3.3V, simplifying design and reducing external components
  - External resistor divider for custom output voltages. 0.6V to 3.8V
- I_{OUT}: 3A Continuous
- 1% Output Voltage Tolerance in PWM
- 16µA Quiescent Current
- Operating Modes:
  - Auto Mode (PFM/PWM) – optimized for battery-powered applications
  - Sleep mode
  - FPWM Mode – ensures low output voltage ripple
  - USM (Ultra Sonic Mode)
- Configurable CCM Switching Frequency: 2MHz to 3MHz with step 0.2MHz
- Power Good Signal: Provides system monitoring capability
- Output Discharge
- Protection Circuitry
  - Under-Voltage Lockout
  - V_{IN} Overvoltage Protection
  - Peak Current Limit
  - Valley Current Limit
  - Short Circuit Protection (Hiccup Mode)
  - Thermal Shutdown

Device Information

P/N	Package	Size
AM32103	TQFN-8	1.8 mm x 1.8 mm x 0.55 mm, pitch 0.5 mm



Typical Application Circuit (Internal Divider)

Table of Contents

1. Pin Configuration

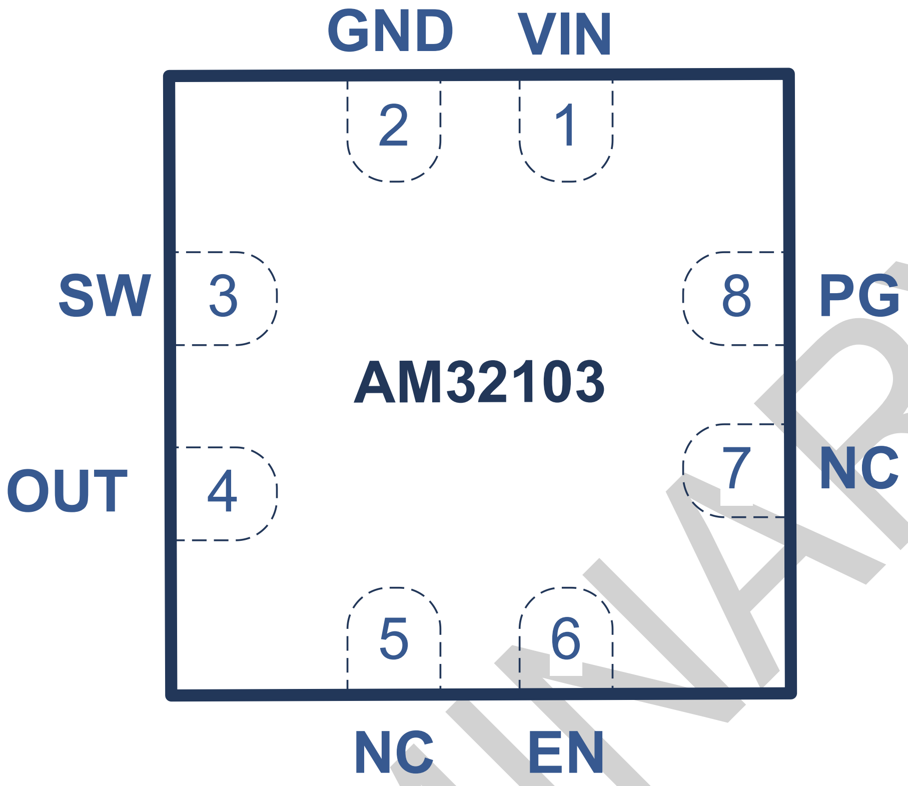


Figure 1-1. Pin Configuration (Top View)

Table 1.1. Pin Description

PIN Number	PIN Name	Function
1	VIN	**Input Voltage**. VIN supplies the power to the IC. Drive VIN with a 2.4V to 5.5V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise due to the switching of the IC.
2	GND	**Power Ground.**
3	SW	**Power Switching Output**. SW is the switching node that supplies power to the output. Connect the external inductor to this pin.
4	OUT	This pin serves as a sense pin for monitoring the output voltage when selecting the internal output voltage. No capacitor is needed near this pin. Please leave as “Not connected” when the external divider is used
5	FB	**Feedback sensing terminal for the output voltage.** Connect this pin to the resistive divider of the output. Please leave as “Not connected” when the internal divider is used.
6	EN	**Enable Input**. EN is a digital input that turns the regulator ON or OFF. Drive EN high to turn ON the regulator and low to turn it OFF. Do not leave as floating.
7	NC	**Not Connected.** NC is floating.
8	PG	**Power Good**. Open drain power-good output that is pulled to GND when the output voltage is out of regulation or during soft-start.

1. Ordering Information

The base part number is always **AM32103**. It is followed by a sequence of characters that define the specific configuration of the device. The order of these parameters is fixed and must be followed exactly:

Table 1.1. Part Number Decoding

Base Part Number	Switching Frequency (MHz)	Voltage Divider	Operation Mode
AM32103	2.0, 2.2, 2.4, 2.6, 2.8, 3.0	06, 09, 11, 18, 25, 33, XX	A, F, U

- **Switching Frequency: *20*** = 2.0 MHz, ***22*** = 2.2 MHz, ***24*** = 2.4 MHz, ***26*** = 2.6 MHz, ***28*** = 2.8 MHz, ***30*** = 3 MHz
- **Voltage Divider: *06*** = 0.6V, ***09*** = 0.9V, ***11*** = 1.1V, ***18*** = 1.8V, ***25*** = 2.5V, ***33*** = 3.3V, ***XX*** = External divider
- **Operation Mode: *A*** = Auto, ***F*** = FPWM, ***U*** = USM

The full part number follows this format:
AM32103 + (Switching Frequency) + (Voltage Divider) + (Operation Mode)

Table 1.2. Part Number Configurations

Part Number	Switching Frequency	Voltage Divider	Operation Mode
AM3210320XXA	2	External divider	Auto
AM3210320XXF			FPWM
AM3210320XXU			USM
AM3210330XXA	3		Auto
AM3210330XXF			FPWM
AM3210330XXU			USM
AM321032009A	2	0.9V(Internal Divider)	Auto
AM321032009F			FPWM
AM321032009F			USM
AM321033009A	3		Auto
AM321033009F			FPWM
AM321033009U			USM
AM321032011A	2	1.1V(Internal Divider)	Auto
AM321032011F			FPWM
AM321032011U			USM
AM321033011A	3		Auto
AM321033011F			FPWM
AM321033011U			USM
AM321032018A	2	1.8V(Internal Divider)	Auto
AM321032018F			FPWM
AM321032018U			USM
AM321033018A	3		Auto
AM321033018F			FPWM
AM321033018U			USM
AM321032033A	2	3.3V(Internal Divider)	Auto
AM321032033F			FPWM
AM321032033U			USM
AM321033033A	3		Auto
AM321033033F			FPWM
AM321033033U			USM

Note 1. There are 126 unique part numbers based on the different possible configurations of frequency, voltage divider, and mode options.

2. Electrical Specifications

2.1. Absolute Maximum Conditions

Table 2.1. Absolute Maximum Conditions

Parameter	Parameter	Min.	Max.	Unit
V_{IN}	Power Input Voltage	-0.3	7.0	V
V_{FB}	Feedback Voltage	-0.3	VIN + 0.3	V
V_{SW_DC}	Switch Node (DC)	-0.3	VIN + 0.3	V
T_{ST}	Storage Temperature	-65	150	°C
T_J	Junction Temperature	--	150	°C
T_L	Lead Temperature	--	260	°C
HBM	ESD Protection (Human Body Model)	--	+/-2000	V
CDM	ESD Protection (Charged Device Model)	--	+/-1300	V
MSL	Moisture Sensitivity Level	1		

Note 2. Stresses greater than the Absolute Maximum Ratings specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods.

Note 3. Semiconductor devices are ESD-sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

2.2. Thermal Resistance

Table 2.2. Thermal Resistance

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction to Ambient	65	°C/W

2.3. Recommended Operating Conditions

Table 2.3. Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Input Voltage	2.4	5.5	V
V_{OUT}	Output Voltage	0.6	3.8	V
I_{OUT}	Output Current	0	3	A
T_A	Operating Ambient Temperature	-40	85	C
T_J	Operating Junction Temperature	-40	125	C

Note 4. The device function is not guaranteed outside of the recommended operating conditions.

2.4. Electrical Characteristics

@ V_{IN} = 2.4V to 5.5V, T_A= - 40 °C to +85 °C. Typical values are at T_A = 25°C and V_{IN} = 5V (unless otherwise noted)

Table 2.4. Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
Current Consumption						
I_{SHDN}	Shutdown Current	EN = LO	0.005	0.05	1.6	µA
I_Q	Quiescent Current	EN = HI, no load, no switching	2.5	15.1	35	µA
Switch FET Resistance						
R_{HS}	High-side FET on Resistance	I_{LOAD}=10mA	32.1	40	49	mΩ
R_{LS}	Low-side FET on Resistance	I_{LOAD}=10mA	9.6	14.6	19.5	mΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
Power Good and Soft-start						
V_{PG}	Power Good Lower Threshold (% of Output Regulation)	V_{FB} Falling	88.4	89.9	91.6	%
		V_{FB} Rising	95	96.5	98	%
	Power Good Upper Threshold (% of Output Regulation)	V_{FBT} Rising	109.8	111	113	%
		V_{FB} Falling	103.5	104	106	%
	Power Good Output Logic Low	I_{PG} = -50uA	--	--	30u	V
t_{PG_EN}	Power good deglitch delay during operation	High-to-low or low-to-high transition on the PG pin	--	40	--	µs
t_{SS}	Soft-start time (5)		0.34	0.49	0.61	ms
$t_{d(EN)}$	Enable Delay Time (5)	VIN = HIGH, EN is rising	0.5	0.7	1.3	ms
$t_{d(PG)}$	Power Good Delay at Start-Up (3)	Low to High PG during Start-Up	34	43	49	µs
Output Voltage						
V_{OUT}	Output Voltage Accuracy	Internal Divider 1.1V, PWM mode	-1%	1.1	+1%	V
		Internal Divider 1.8V, PWM mode	-1%	1.8	+1%	V
		Internal Divider 2.5V, PWM mode	-1%	2.5	+1%	V
		Internal Divider 3.3V, PWM mode	-1%	3.3	+1%	V
Switch Frequency						
F_{SW}	PWM Switching Frequency	IOUT = 1A, VOUT = 1.8V(Internal)	-10%	2	+10%	MHz
			-10%	3	+10%	
EN Digital Logic						
V_{EN_H}	EN Logic High Threshold		0.74	--	--	V
V_{EN_HYS}	EN Logic Hysteresis		--	40	--	mV
Protection Features						
I_{HS_Limit}	HS Peak Current Limit (6)	From Source to Drain	--	5.7	--	A
I_{LS_Limit}	LS Valley Current Limit (6)	From Source to Drain	--	3.2	--	
V_{OVP}	Overvoltage Protection, Rising	V_{OVP_RISING}	6.11	6.34	6.56	V
	Overvoltage Protection, Hysteresis	V_{OVP_HYS}	251	280	300	mV
V_{UVLO}	Undervoltage Protection, Rising	V_{UVLO_RISING}	2.23	2.3	2.38	V
	Undervoltage Protection, Hysteresis	V_{UVLO_HYS}	--	100	--	mV
T_{SD}	Thermal Shutdown (Junction Temperature)		150	153	155	°C
T_{HYS}	Thermal Shutdown Hysteresis		25	27	28	°C
R_{DIS}	Output Discharge Resistor		130	137	145	Ω

Note 5. $t_{d(EN)}$ measure between V_{EN_H} and V_{OUT_TARGET}*10%.

Note 6. $t_{d(PG)}$ measure between V_{OUT_TARGET}*95% and V_{PG_TARGET}*10%.

Note 7. Compliance with the datasheet limits is ensured through one or more approaches, including production testing, characterization, and/or design verification.

3. Typical Characteristics

3.1. Typical Electrical Characteristics

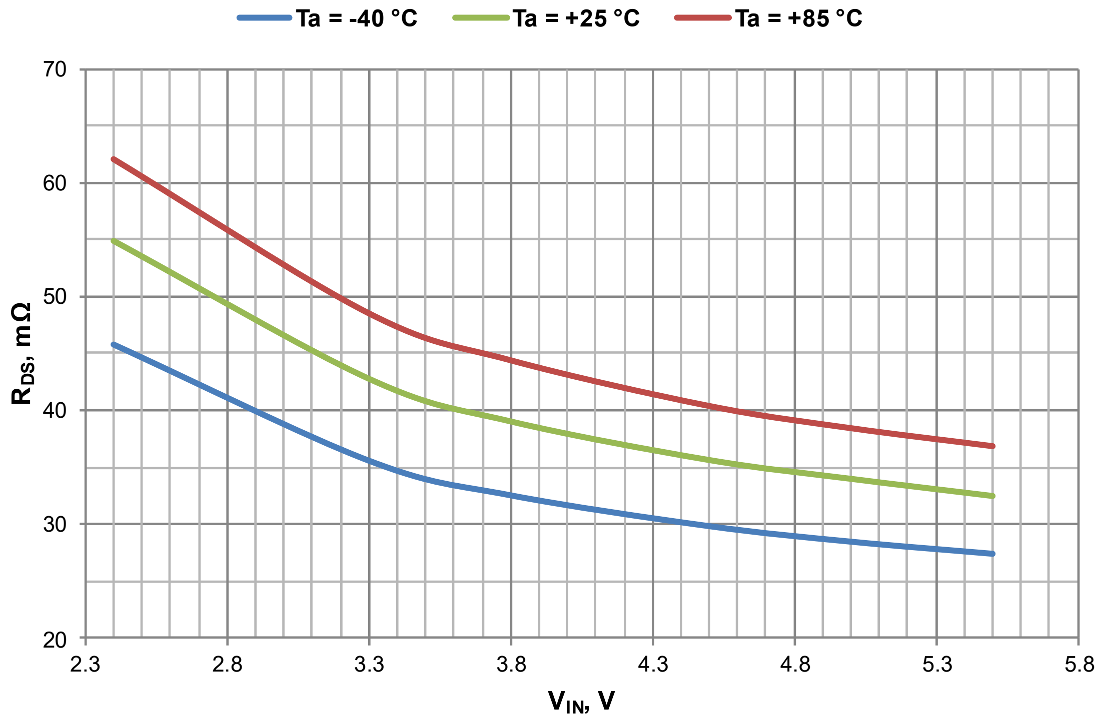


Figure 3-1. High Side FET On-Resistance

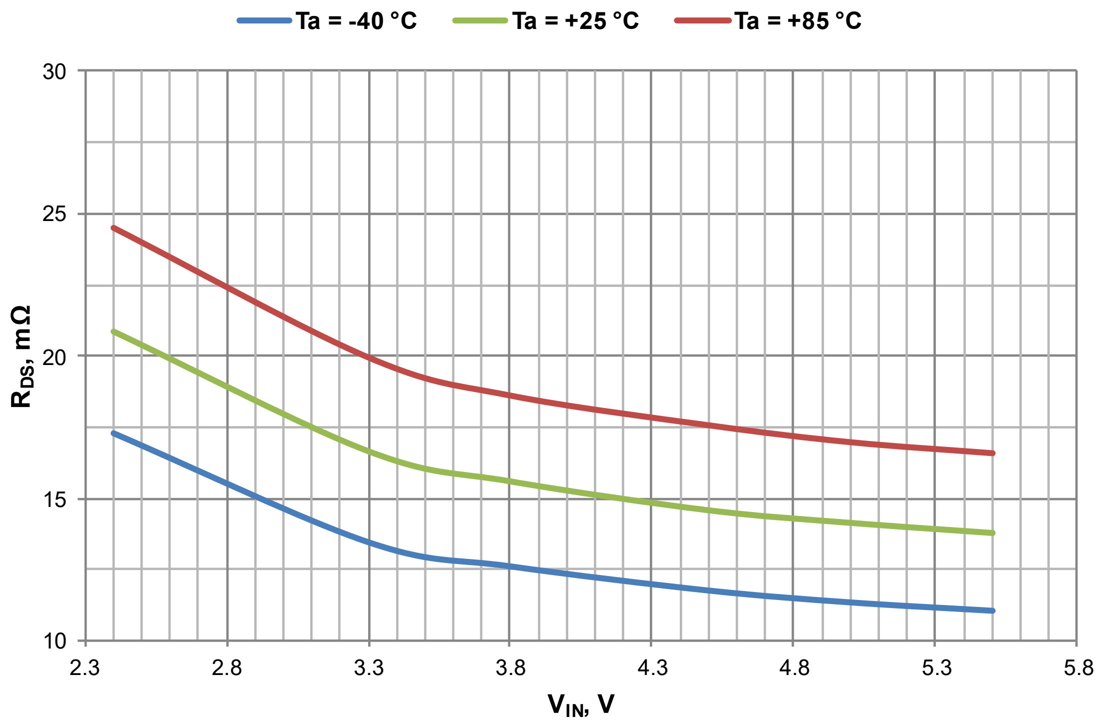


Figure 3-2. Low Side FET On-Resistance

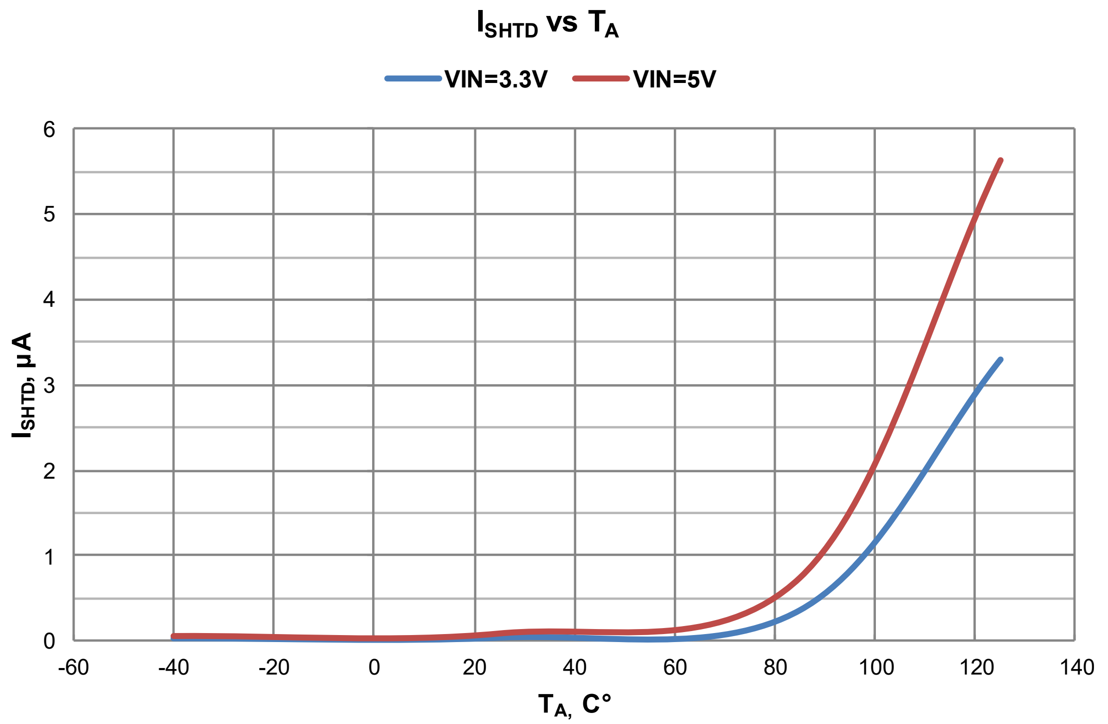


Figure 3-3. Shutdown Current

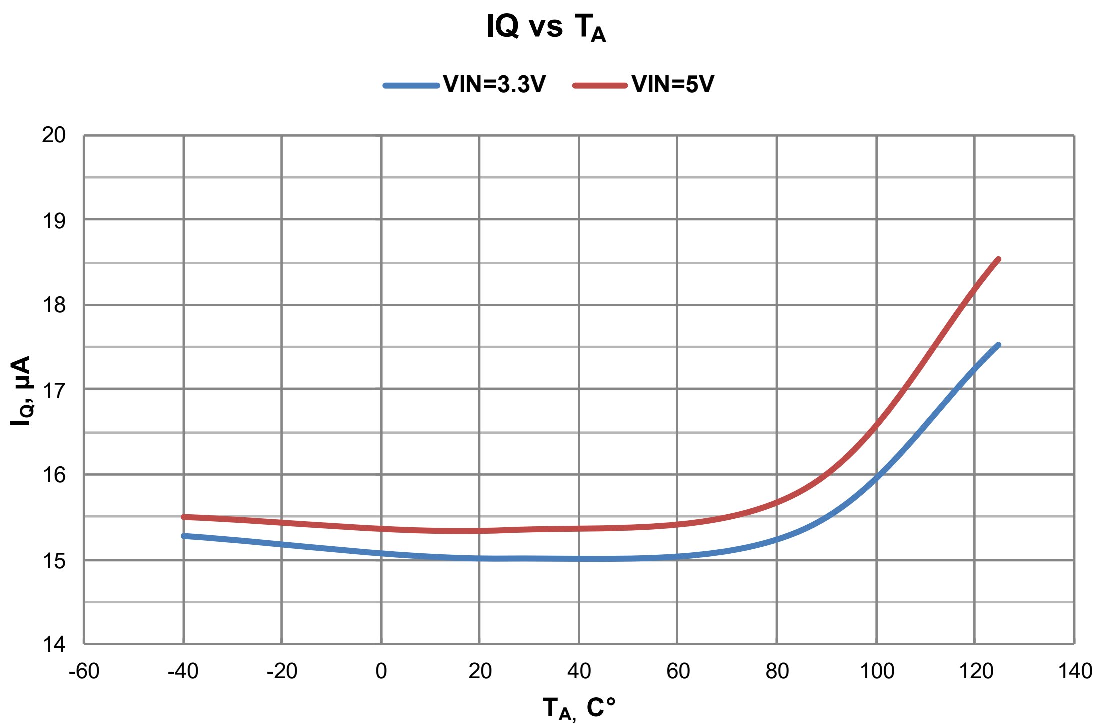


Figure 3-4. Quiescent Current

3.2. Typical Performance Characteristics

Conditions: L=470nH, DCR=22mΩ, C_{IN}=22µF+22µF+47µF, C_{OUT}=22µF, F_{SW} = [2MHz, 3MHz] in PWM.

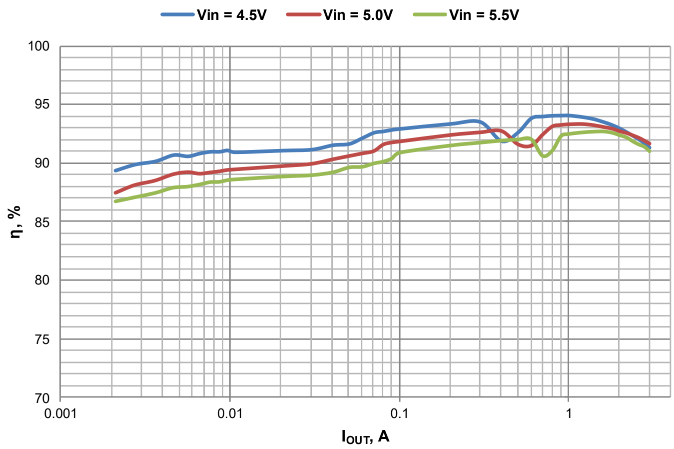


Figure 3-5. Efficiency vs Load, F_{SW}=2MHz AUTO, V_{OUT}=3.3V

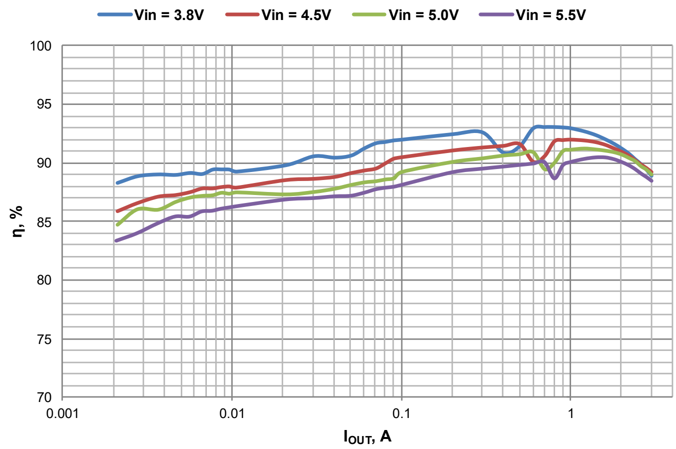


Figure 3-6. Efficiency vs Load, F_{SW}=2MHz AUTO, V_{OUT}=2.5V

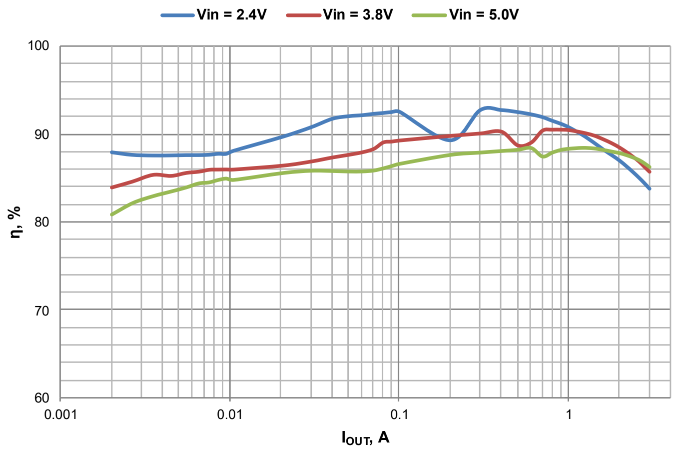


Figure 3-7. Efficiency vs Load, F_{SW}=2MHz AUTO, V_{OUT}=1.8V

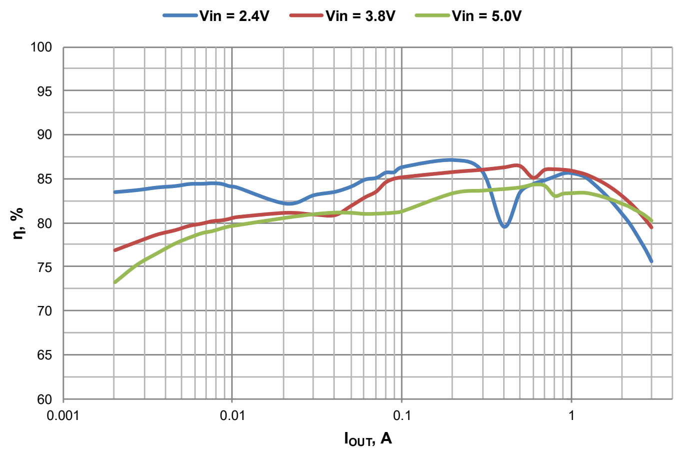


Figure 3-8. Efficiency vs Load, F_{SW}=2MHz AUTO, V_{OUT}=1.1V

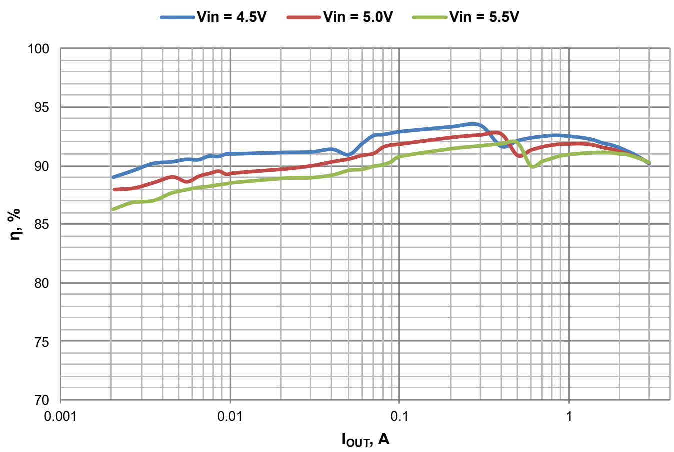


Figure 3-9. Efficiency vs Load, F_{SW}=3MHz AUTO, V_{OUT}=3.3V

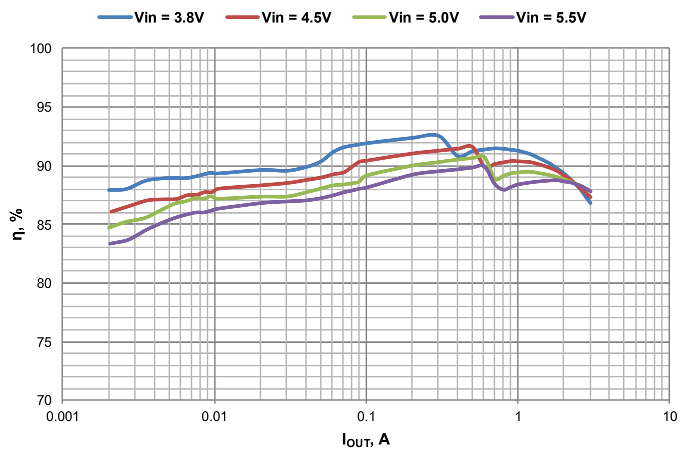


Figure 3-10. Efficiency vs Load, F_{SW}=3MHz AUTO, V_{OUT}=2.5V

INTERNAL Divider, V_{OUT} = 3.3V, F_{SW}=2MHz

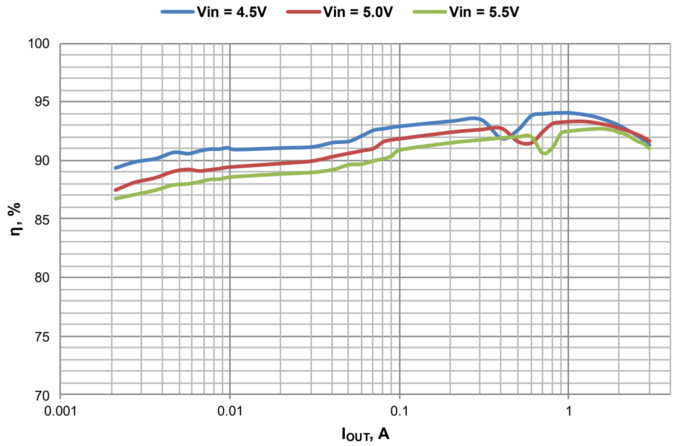


Figure 3-11. Efficiency vs Load, AUTO mode

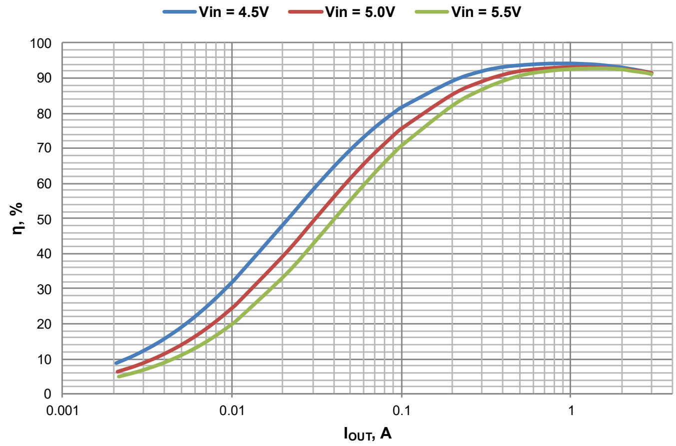


Figure 3-12. Efficiency vs Load, FPWM mode

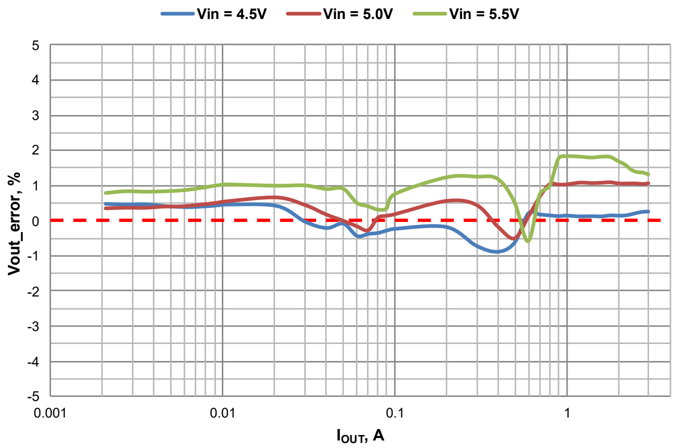


Figure 3-13. Load Regulation, AUTO mode

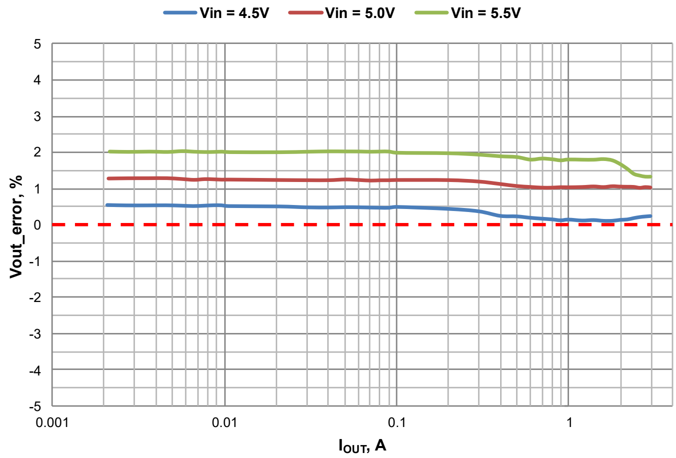


Figure 3-14. Load Regulation, FPWM mode

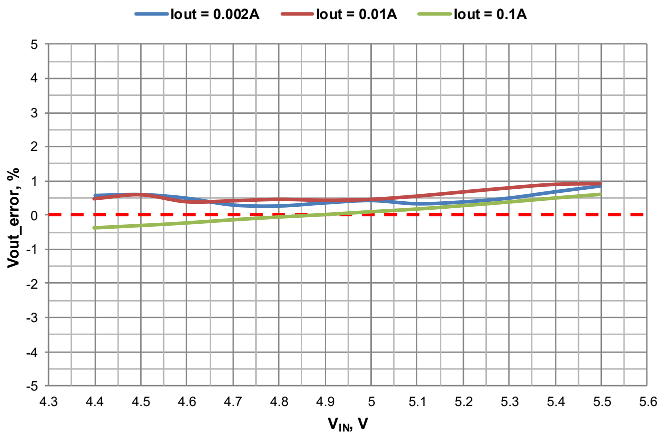


Figure 3-15. Line Regulation, AUTO mode

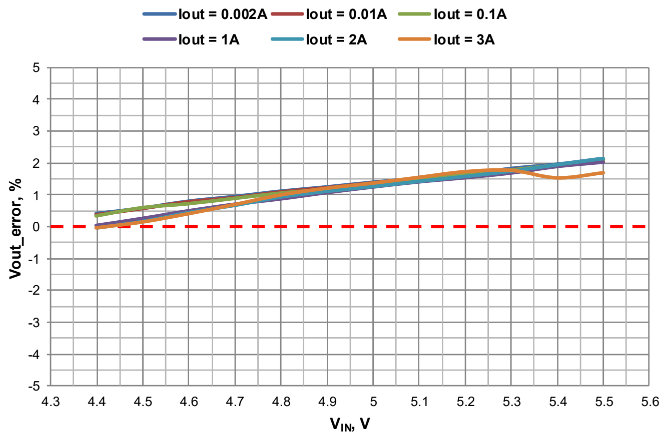


Figure 3-16. Line Regulation, FPWM mode

INTERNAL Divider, V_{IN}=5.0V, V_{OUT} = 3.3V, F_{SW}=2MHz,

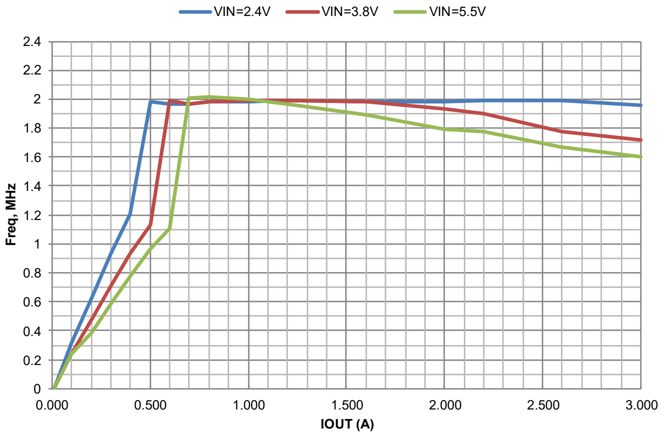


Figure 3-17. F_{SW} VS Load

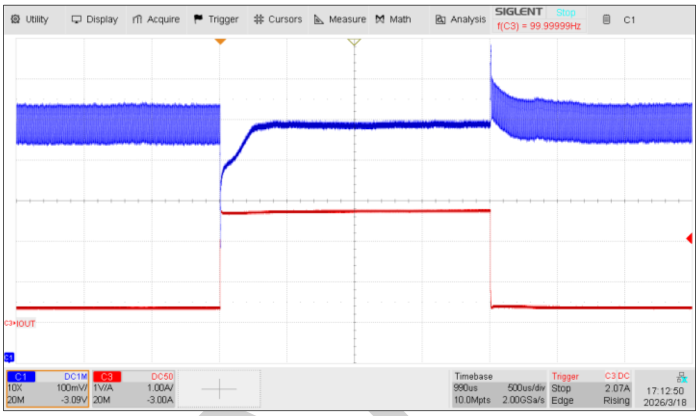


Figure 3-18. Load Transient, Load Slew rate 1A/us

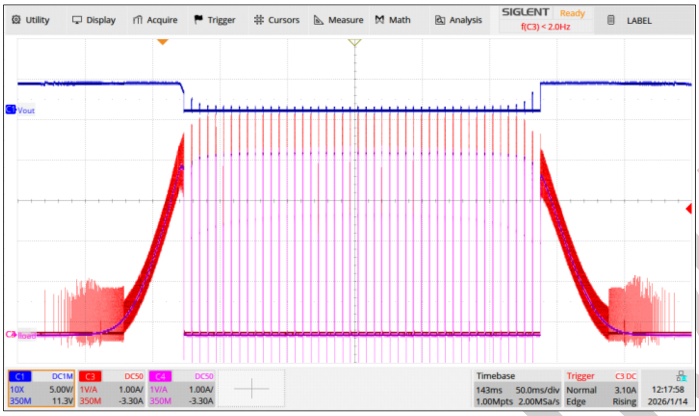


Figure 3-19. Output Short Protection & Hiccup mode

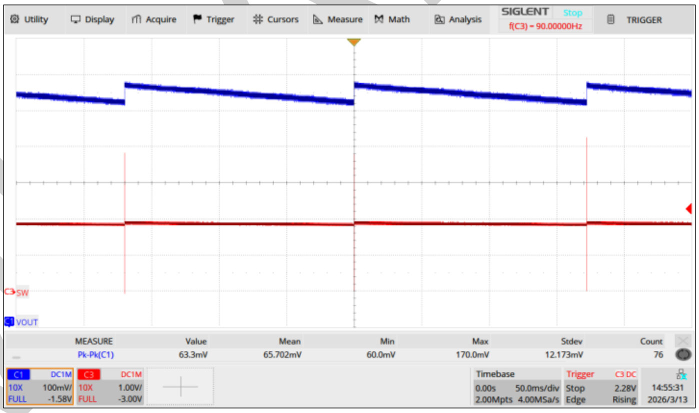


Figure 3-20. V_{OUT} Ripple, Sleep mode, Load =0A

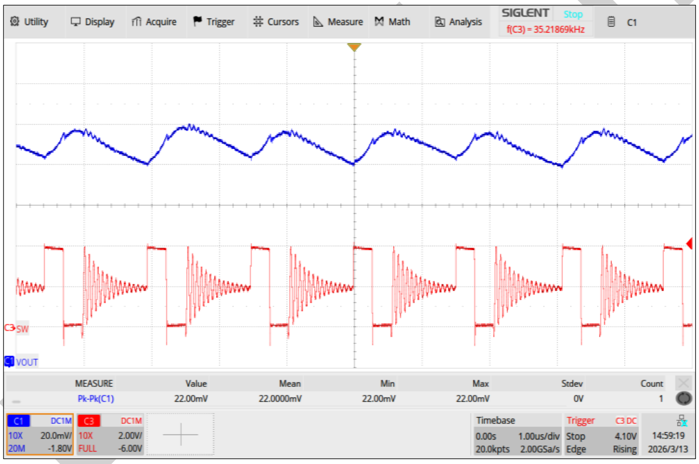


Figure 3-21. V_{OUT} Ripple, Sleep mode Disable

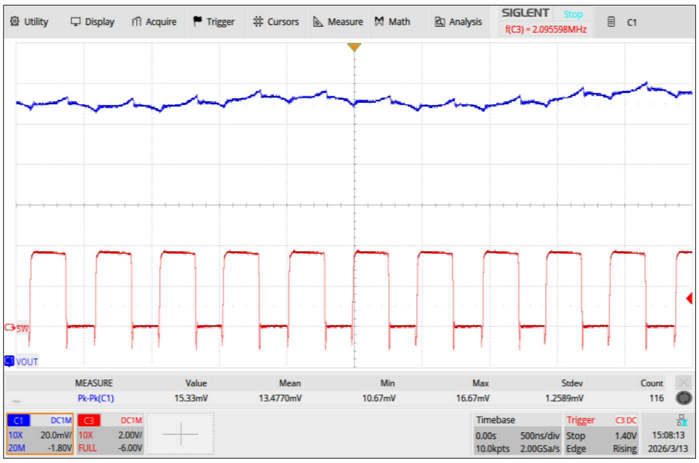


Figure 3-22. V_{OUT} Ripple, PWM mode Load=3A

INTERNAL Divider, V_{OUT} = 1.8V, 2MHz

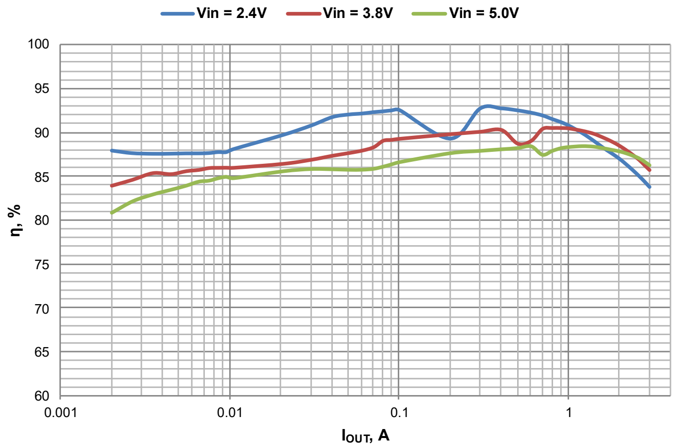


Figure 3-23. Efficiency vs Load, AUTO mode

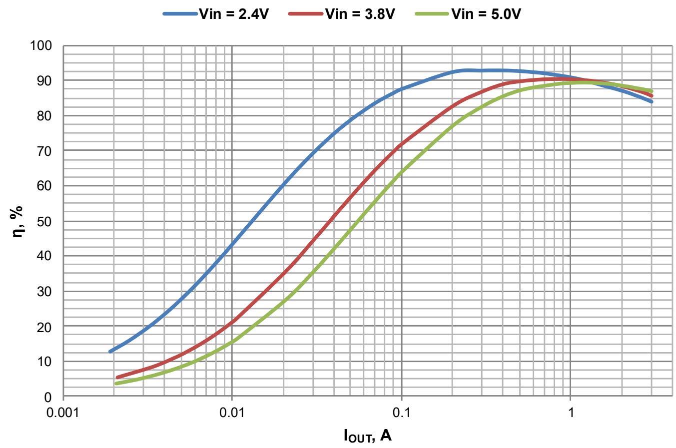


Figure 3-24. Efficiency vs Load, FPWM mode

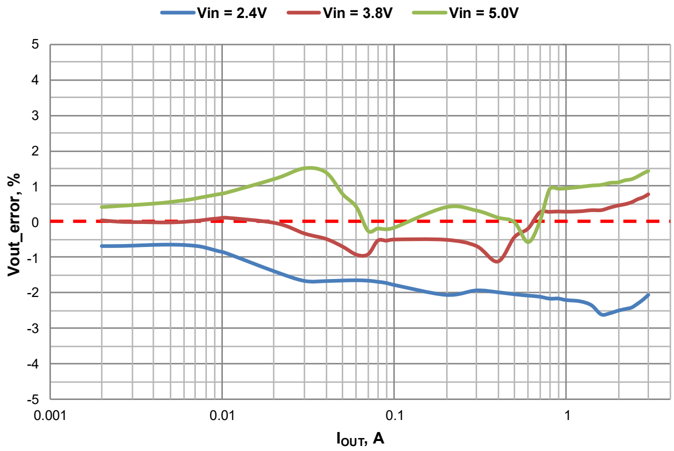


Figure 3-25. Load Regulation, AUTO mode

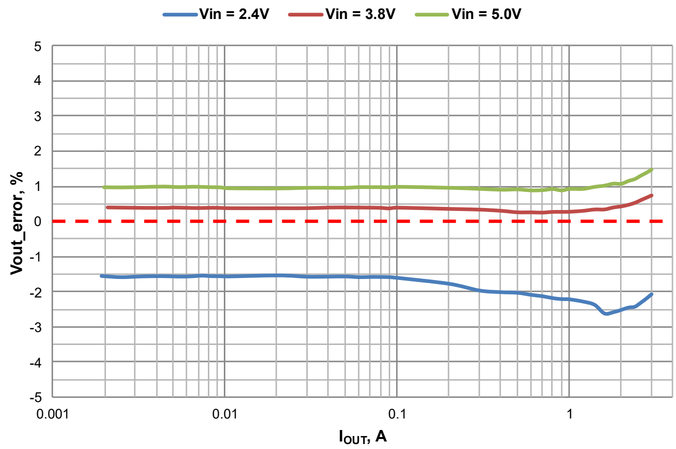


Figure 3-26. Load Regulation, FPWM mode

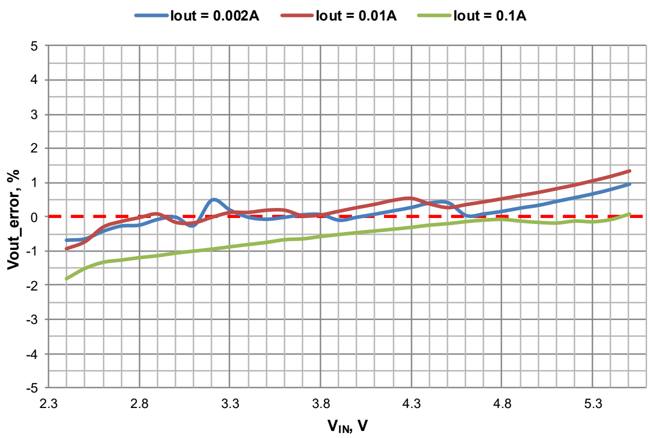


Figure 3-27. Line Regulation, AUTO mode

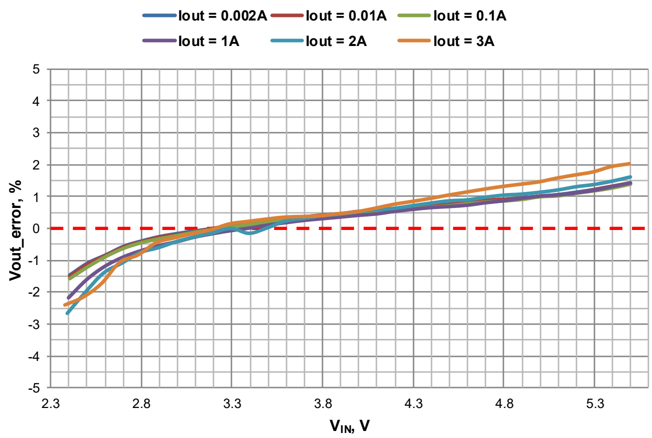


Figure 3-28. Line Regulation, FPWM mode

INTERNAL Divider, V_{OUT} = 1.8V, 2MHz

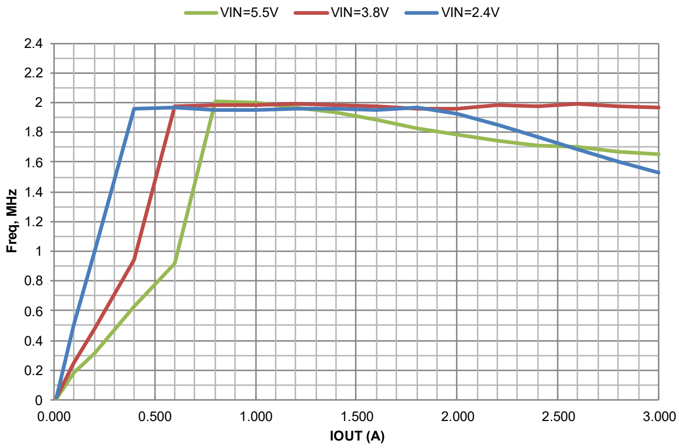


Figure 3-29. F_{SW} vs Load, AUTO mode

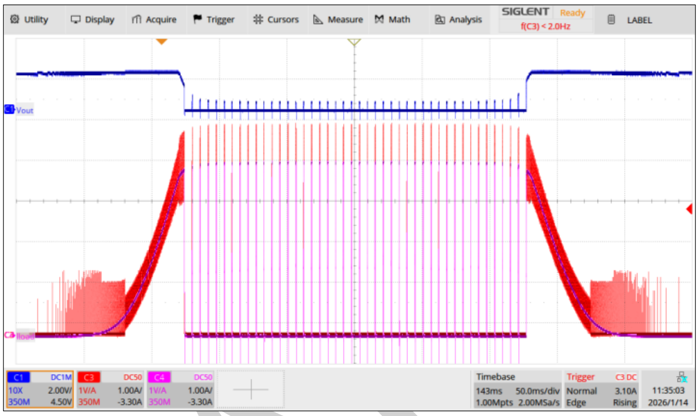


Figure 3-30 Output Short Protection & Hiccup mode

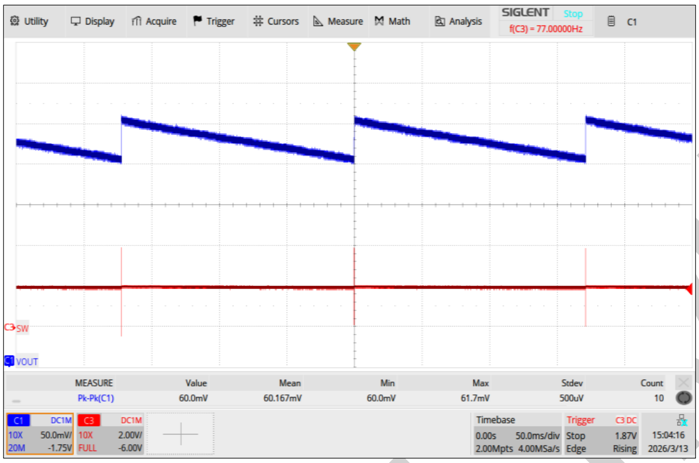


Figure 3-31. V_{OUT} Ripple, Sleep mode, Load =0A

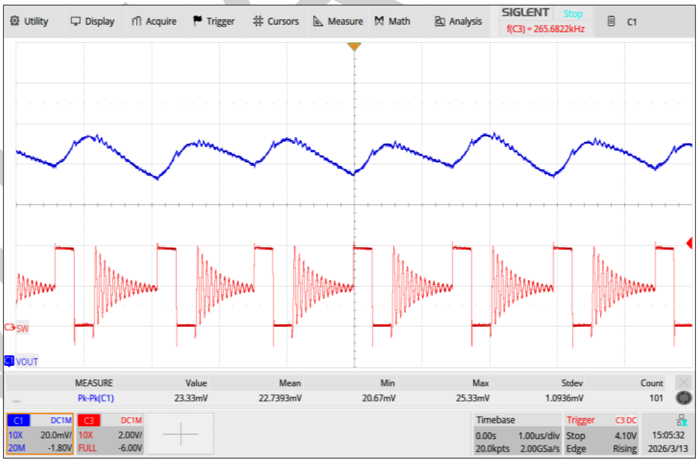


Figure 3-32. V_{OUT} Ripple, PFM mode, Load =0.2A

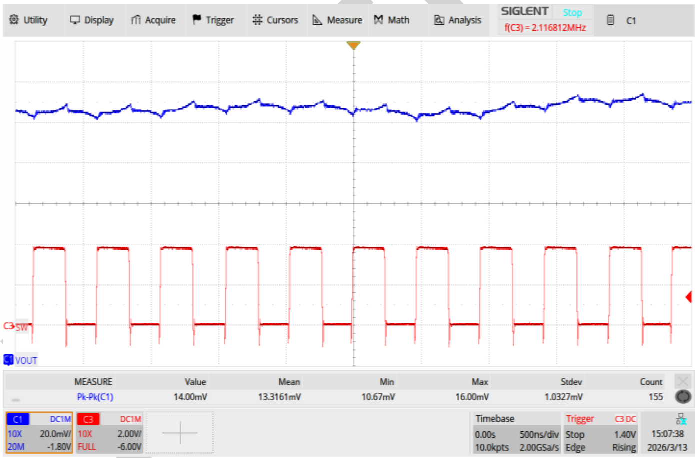


Figure 3-33. V_{OUT} Ripple, PWM mode, Load =3A

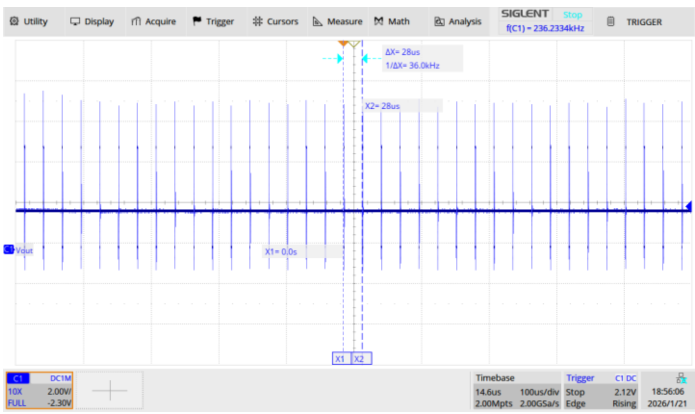


Figure 3-34. USM mode

INTERNAL Divider, V_{OUT} = 1.8V, 2MHz

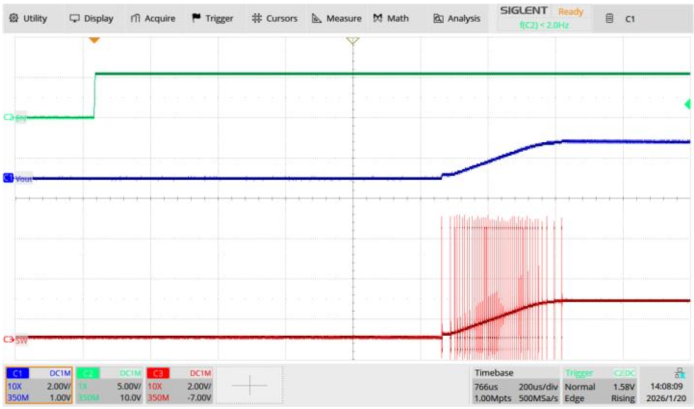


Figure 3-35. Start-up, VIN=5.5V, Load=0A

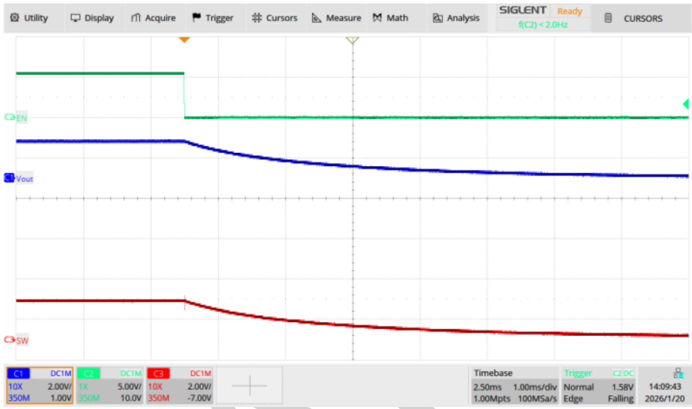


Figure 3-36. Shutdown, VIN=5.5V, Load=0A

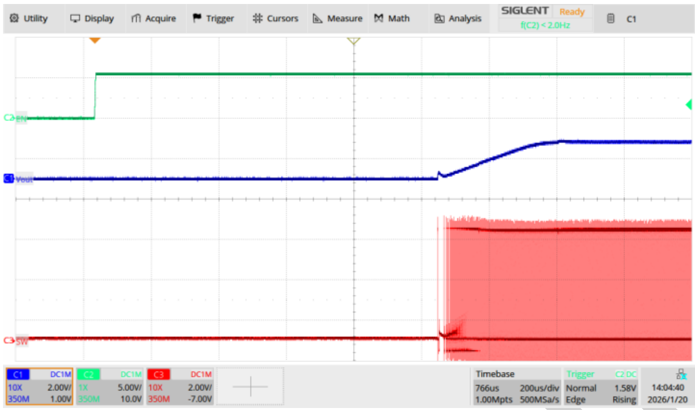


Figure 3-37. Start-up, V_{IN}=5.5V, Load=2A

Figure 3-38. Shutdown, V_{IN}=5.5V, Load=2A

4. Functional Description

4.1. Control Architecture

The AM32103 is a highly efficient, synchronous buck converter with integrated power transistors. It is designed for a wide range of applications, offering programmable operating modes to suit different load conditions. For light loads, it operates in Pulse-Frequency Modulation (PFM) mode, optimizing efficiency and minimizing current consumption. For medium and heavy loads, it switches to Pulse Width Modulation (PWM) mode, which helps reduce output ripple. Additionally, the AM32103 features a forced PWM mode, which ensures low ripple independent of the load, making it ideal for noise-sensitive applications.

The AM32103 allows users to program key parameters such as PWM frequency (2 MHz to 3 MHz) and output voltage levels. During mass production or large-volume sampling, the required configurations are programmed during factory testing, ensuring that the device arrives pre-configured to meet user specifications.

For detailed information on all features and settings, please refer to the following subsections.

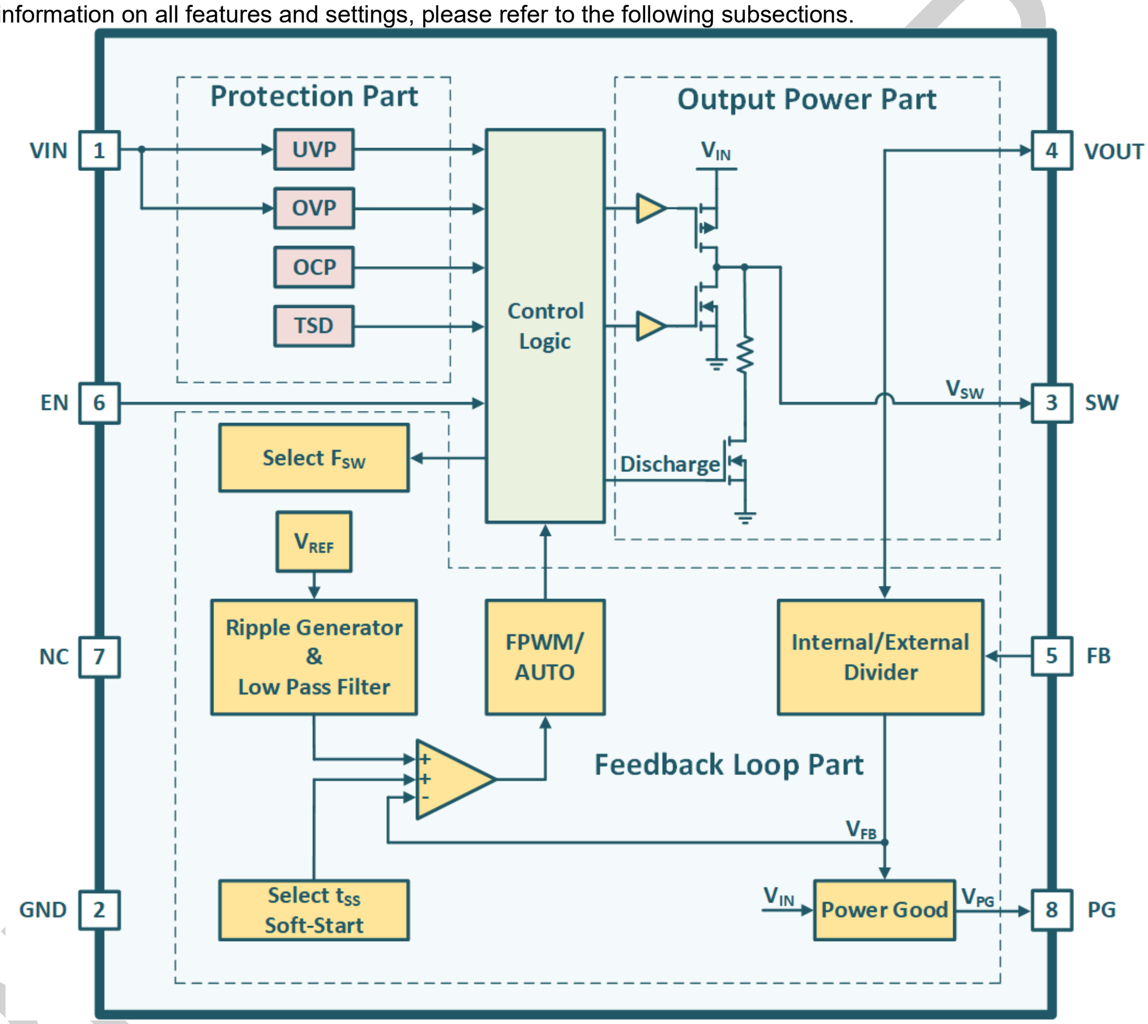


Figure 4-1. Functional Block Diagram

4.1.1. Adaptive Constant On-Time

The AM32103 is an adaptive constant-on-time, synchronous step-down converter. An adaptive on-time control scheme is employed for a constant switching frequency irrespective of input voltage, simplifying control scheme.
During steady-state operation the V_{FB} amplifier senses the feedback voltage and compares to the voltage reference. When the feedback voltage falls below the reference voltage the on-time period is triggered.
During a change in load transient the constant-on-time architecture will modify the switching frequency (T_{OFF} varies) but return to nominal fixed frequency once V_{OUT} has stabilized.

4.1.2. PFM Mode

When the load drops below half of the peak-to-peak current of the inductor, Discontinuous Conduction Mode (DCM) is activated, and the switching frequency becomes variable; the lower the load, the lower the frequency. The on-time still depends on the ratio of the output to input voltage. Still, during the remaining time, the power transistors are off, and only the output capacitor provides the output voltage. The next switching cycle begins when the voltage at the feedback loop falls below the reference voltage.

4.1.2.1. Sleep Mode

In Sleep Mode, the IC operates similarly to DCM but at reduced switching frequencies. A low-power sleep comparator replaces the main comparator to reduce power consumption. This improves efficiency at light loads, but results in increased output voltage ripple and degraded line regulation compared to DCM with Sleep Mode disabled.

Note 8. During Sleep Mode, the Thermal Shutdown is OFF

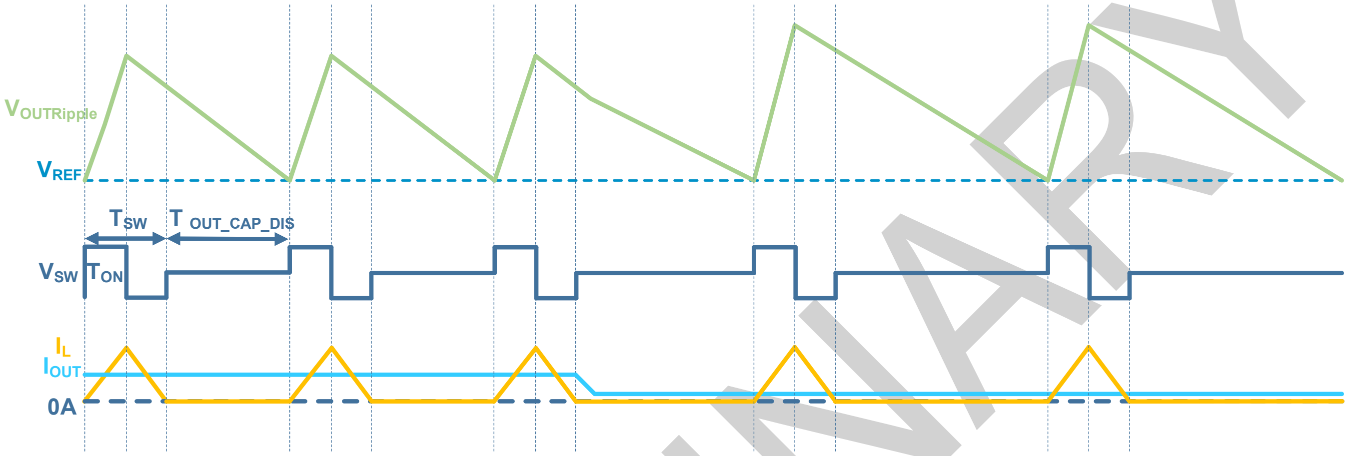


Figure 4-2. Adaptive COT during Steady-State (PFM) Light Loads

4.1.2.2. Ultrasonic Mode

The ultrasonic mode (USM) is an optional control feature that maintains a switching frequency above the audible range at low load conditions. When enabled, this feature maintains a frequency higher than the audible frequency range by adding small switching pulses. This mode leads to improved low-load regulation at the tradeoff of greater quiescent current.

Table 4.1. Ultrasonic mode. Limit

Signal Function	Min.	Typ.	Max.	Unit
Ultrasonic mode	54	60	66	kHz
	25	30	37	kHz

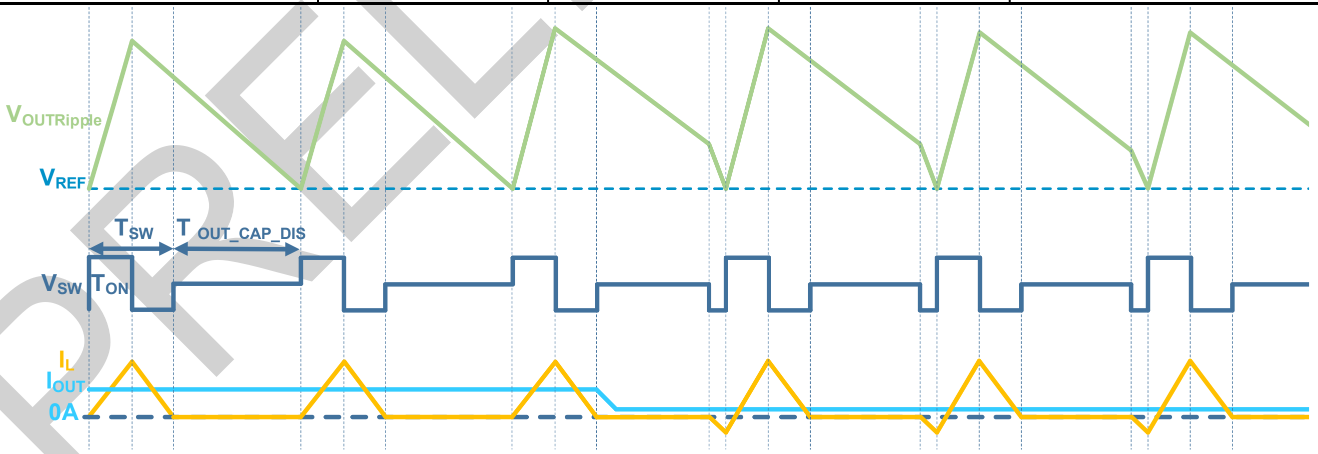


Figure 4-3. Ultrasonic Mode

Note 9. The USM mode is disabled by default.

Note 10. The USM mode is suitable when duty cycle < 70%.

4.1.3. PWM Mode

When the load exceeds half of the peak-to-peak current of the inductor, it indicates Continuous Conduction Mode (CCM), and the converter adjusts the pulse width while keeping the frequency stable in the steady state.

Please review the two formulas below: the first calculates the constant on-time in CCM mode, and the second determines the transition point from Discontinuous Conduction Mode (DCM) to CCM.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \cdot F_{SW}} \quad (1)$$

Where,

- V_{OUT} – output voltage (V)
- V_{IN} – input voltage (V)
- F_{SW} – switching frequency (Hz)

$$I_{LOAD} = \left(\frac{V_{IN} - V_{OUT}}{2L}\right) \cdot T_{ON} \quad (2)$$

Where,

- L – inductor value (H)

The second formula shows that the transition point depends on the inductance. Therefore, caution must be exercised when selecting a small inductance, as a compromise between inductance and DCR (Direct Current Resistance) is always necessary.

Please review the time diagrams below for better understanding:

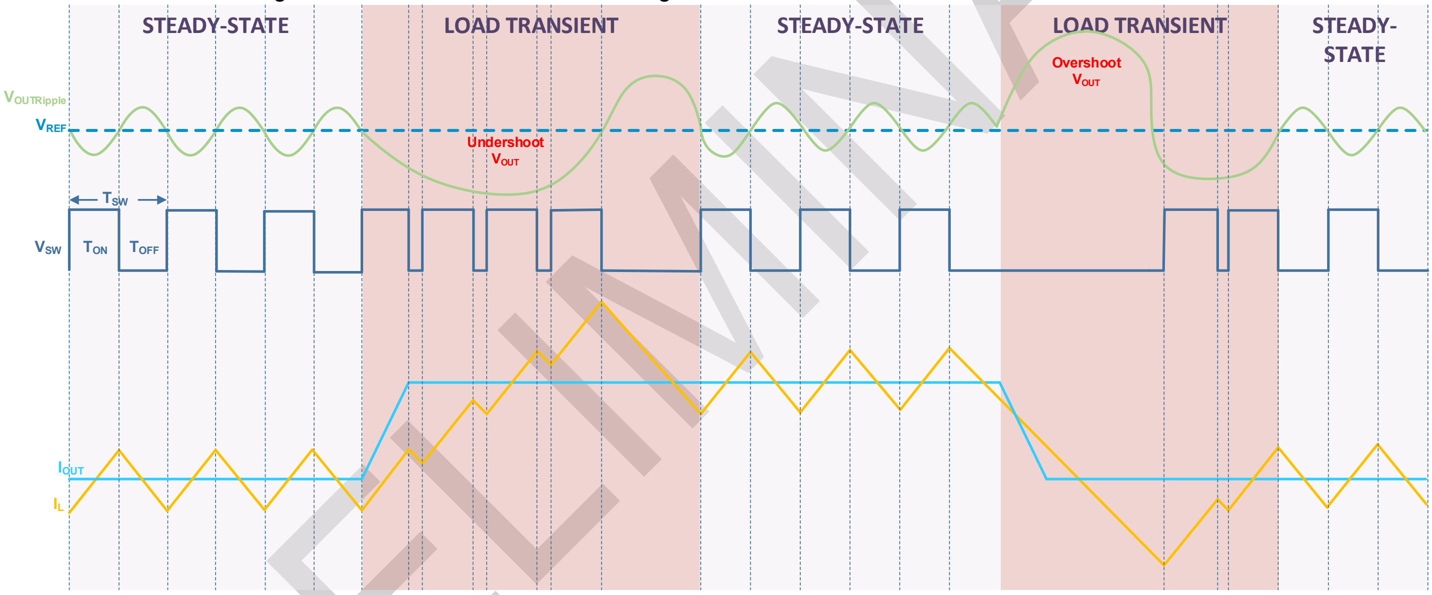


Figure 4-4. Adaptive COT during Steady-State (PWM) and Load Transient events, Middle-Heavy Loads

From the timing diagram above, during the transition process, the on-time is constant while the off-time varies, which in turn changes the frequency.

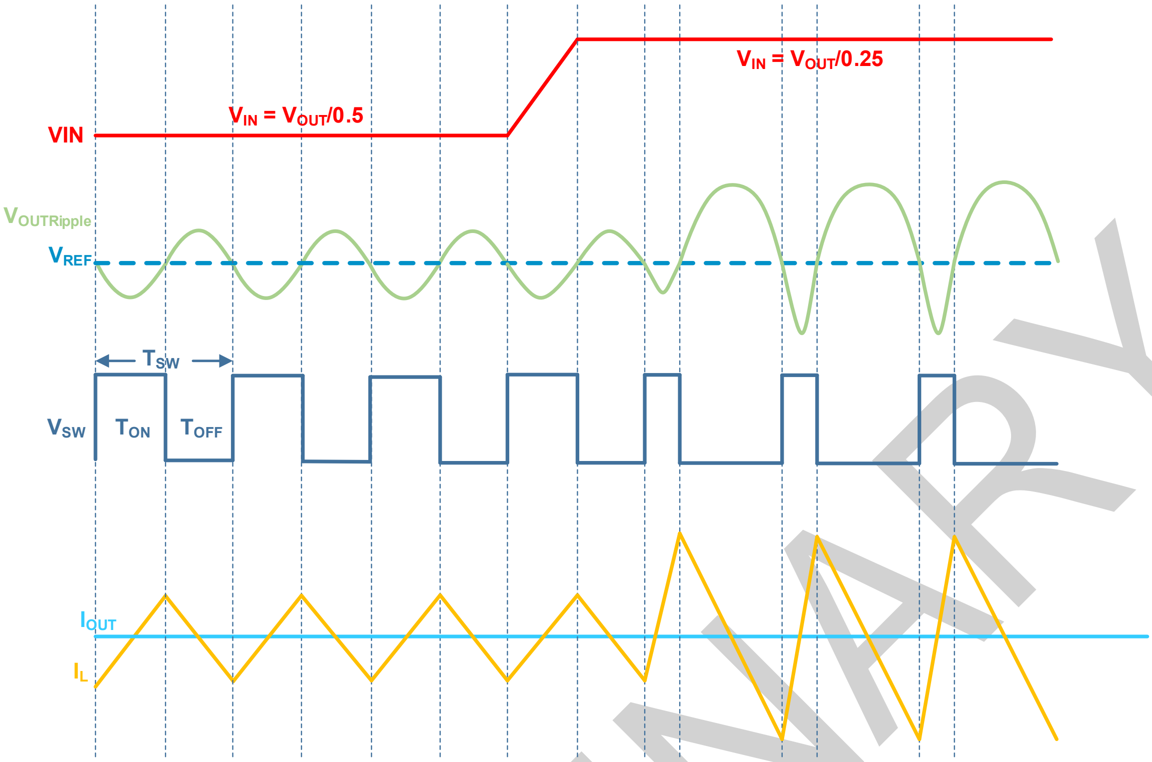


Figure 4-5. Adaptive COT during Steady-State (PWM) V_{IN} changing

The timing diagrams above illustrate how the Constant-ON Time adapts to the ratio of V_{OUT}/V_{IN}.

4.1.3.1. Forced PWM mode

Forced-PWM mode is a configurable option for the AM32103. In this mode, the AM32103 will stay in PWM mode regardless of output current, thereby maintaining a constant switching frequency but increasing quiescent current consumption at lower output current. The AM32103 can be set into forced PWM mode by configuring the non-volatile memory or when the EN pin receives a logic high voltage that is less than V_{IN} – 250 mV.

AM32103 has 3 configurations:

- **FPWM Always Enabled** - PWM is enabled via non-volatile memory. The device maintains a constant switching frequency regardless of load.
- **FPWM Enabled via EN pin** - when the EN pin receives a logic high voltage that is less than VIN – 250 mV.
- **FPWM Disabled** - The FPWM function can now be entirely disabled, meaning the device operates in auto mode only, transitioning between PWM and PFM as needed based on load conditions. This mode results in improved efficiency at light loads due to reduced switching activity. Disabling FPWM is done by configuration and results in no FPWM behavior, regardless of the EN pin state.

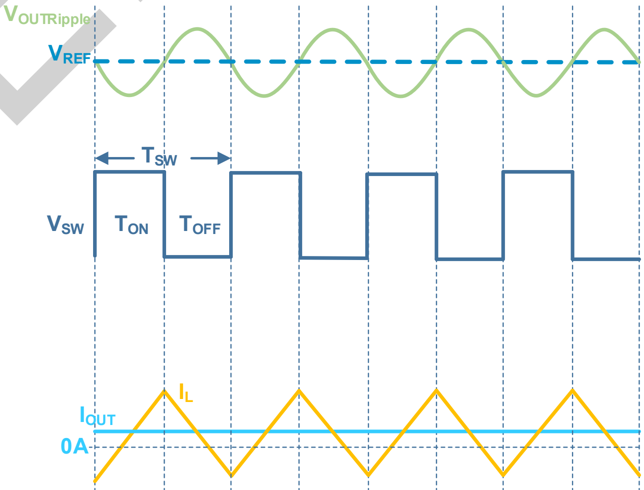


Figure 4-6. FPWM mode

4.2. Enable (EN)

The device is enabled by setting the EN pin to logic HIGH. Conversely, the AM32103 is shut down if the EN pin is pulled low. In shutdown mode, internal control circuitry is turned off, as well as the internal power switches. For the correct operation, do not leave the enable pin floating.
The device operates in PFM mode when the EN pin receives a logic high voltage that is greater than VIN – 250mV. In contrast, the device switches to PWM mode, regardless of the output load, when the EN pin receives a logic high voltage that is less than VIN – 250mV.

Note 11. When feature FPWM is using EN: disabled in NVM, the EN value has no effect.
Note 12. When FPWM is selected in NVM, the EN value has no effect.

4.3. Power Good (PG)

The PG pin of AM32103 is an open-drain output that is actively held low during the soft-start period until the output voltage reaches 95% of its target value. When the output voltage is outside of its regulation by ±10%, PG pulls low until the output returns within 5% of its set value. The PG rising edge transition is delayed by 40μs.

Please see the timing diagram below during the start-up stage.

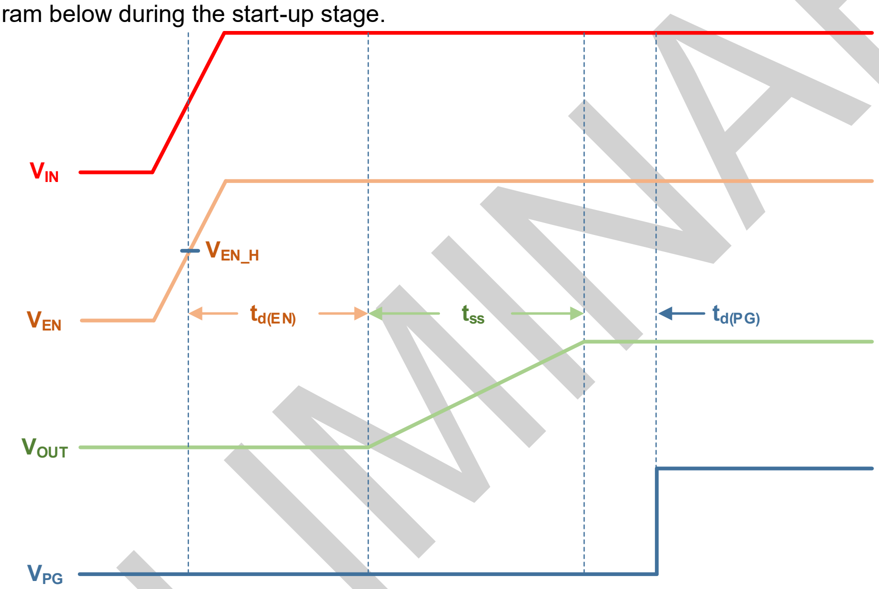


Figure 4-7. Start-Up Timing

4.4. Soft-Start Time

The AM32103 has an optional soft-start configuration for applications that need to reduce in-rush current. If enabled, the soft-start will limit the rate of the output voltage ramp in relation to the chosen soft-start value.
By default, soft-start is 0.5ms. Programmable soft-start options are:

Table 4.2. Soft-Start times

Function	Time	Min.	Typ.	Max.	Unit
Soft start time	Disable	0.044	0.047	0.050	ms
	0.5	0.42	0.46	0.51	
	1.0	0.86	0.91	0.95	
	2.0	1.79	1.92	2.03	

4.5. Protection Mechanisms

4.5.1. Undervoltage Lockout

Undervoltage lockout is implemented to protect the IC from insufficient input voltages. The AM32103 is disabled if the input voltage falls below 2.2V. In this UVLO event, both the high-side and low-side power MOSFETs turn off, and the 140Ω active discharge enables to discharge of the output voltage to the ground. Please see picture below:

Figure 4-8. UVLO Mechanism

Note 1. $V_{EN} = V_{IN}$.

4.5.2. V_{IN} Overvoltage Protection

Similarly, input overvoltage protection is implemented to protect the IC from excess input voltages. The AM32103 disables out if the input voltage rises above 6.3V. In this OVP event, both the high-side and low-side power MOSFETs turn off and the 140Ω active discharge enables the discharge of the output voltage to the ground.

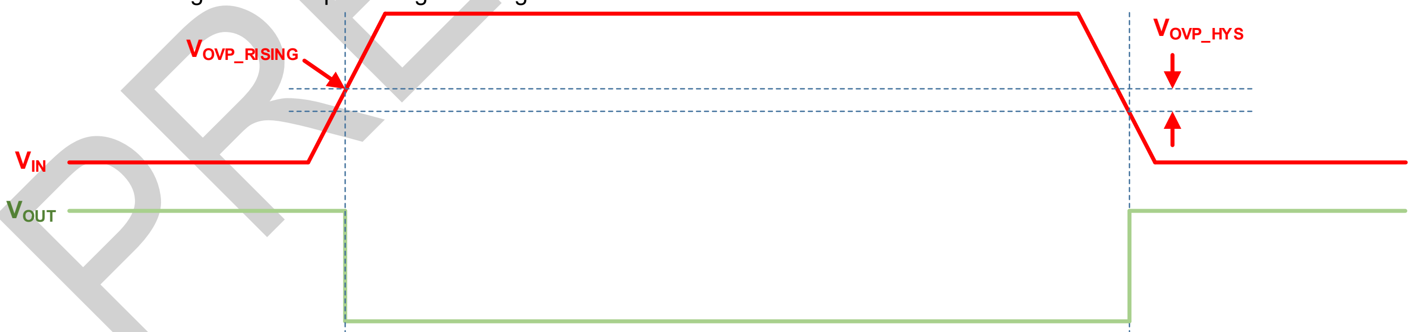


Figure 4-9. OVP Mechanism

Note 2. $V_{EN} = V_{IN}$.

4.5.3. Current Limit

The AM32103 implements cycle-by-cycle current protection by sensing the current through internal MOSFETs.

As the output current gradually increases, see the figure below. When the current through the LS FET exceeds its Valley Current Limit, the LS FET remains on until the inductor current falls back to the limit. Only then can a new high-side on-time start. As the load current continues to rise, the inductor peak-to-peak current increases and the effective switching frequency decreases due to repeated activation of the low valley current limit.

If the output current increases further and the current through the HS FET reaches the High-Side Peak Current Limit, the HS FET is turned off immediately. The LS FET then conducts until the inductor current drops to the low valley limit, after which the HS FET may turn on again. In this condition, the output voltage starts to decrease.
When the feedback voltage (FB) falls to 0.4 V, Output Short Protection is triggered, and the converter enters Hiccup Mode. In Hiccup Mode, the IC waits for 13.6 × Soft-Start time before attempting to restart and ramp up V_{OUT} again. This operation reduces power dissipation during output overcurrent or short-circuit conditions.

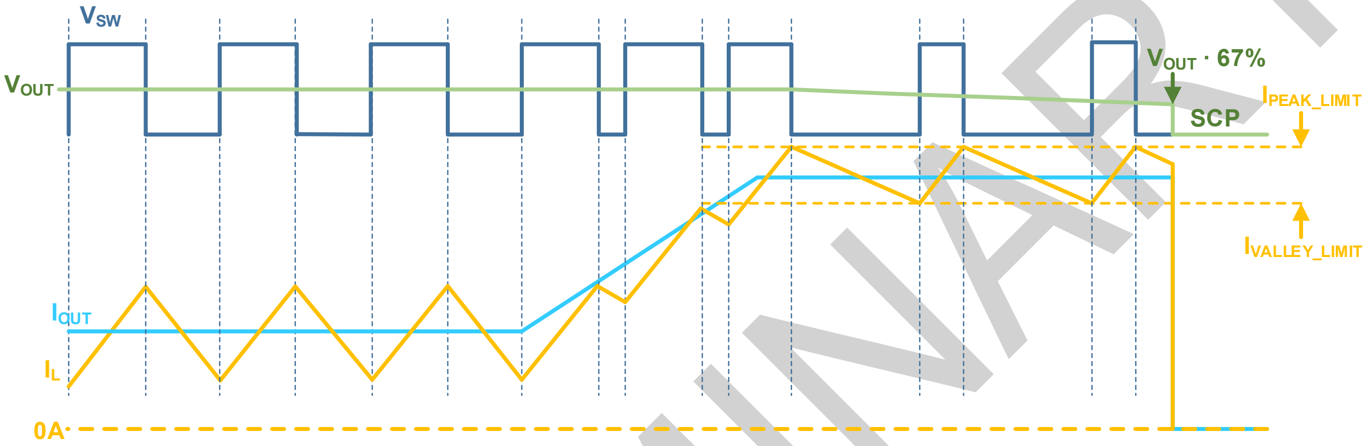


Figure 4-10. Peak, Valley Current Limits, and Hiccup Mode

4.5.4. Thermal Shutdown

If the device's junction temperature reaches the thermal shutdown limit of (+160°C typical), the AM32103 shuts down both its high-side and low-side power MOSFETs. When the junction temperature reduces to the required level (+130°C typical), the device initiates a normal power-up cycle, including soft-start if enabled. Please see the picture below:

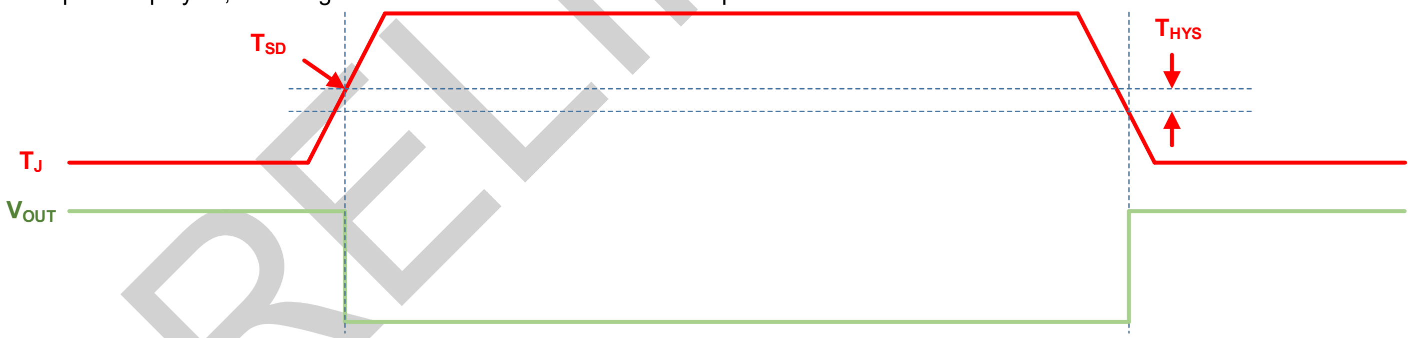


Figure 4-11. Thermal Shutdown Mechanism

5. Application Information

The AM32103 can operate in two configurations: with a pre-selected internal feedback divider, or, if a specific output voltage is required or maximum precision is desired, with an external feedback divider. For more detailed information on component selection, refer to the following subsections.

5.1. Typical Application

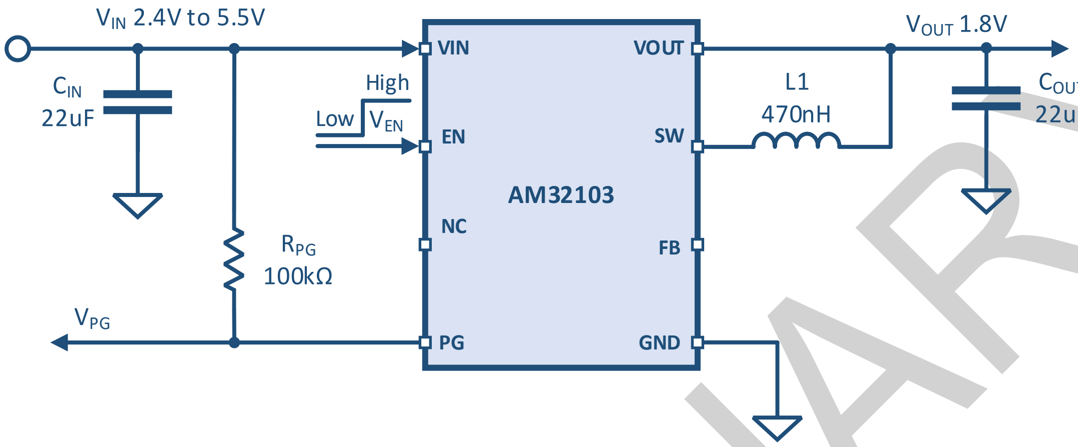


Figure 5-1. Typical Application Circuit for External Divider

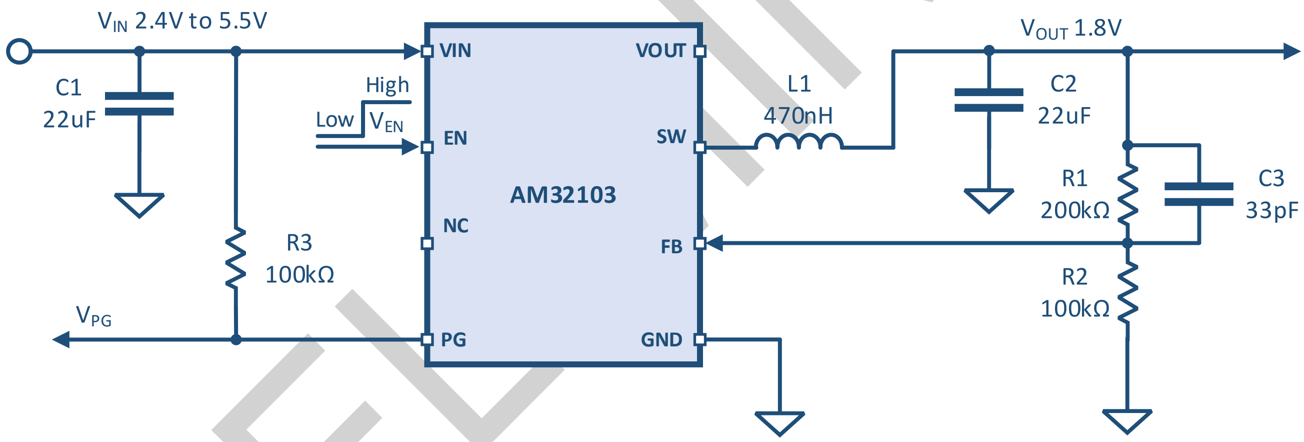


Figure 5-2. Typical Application Circuit for Internal Divider

5.2. Setting the Output Voltage

The AM32103 can select the output voltage in two ways:

5.2.1. Internal Voltage Selection

The output voltage can be selected from a predefined set of internal voltage levels. This method does not require external feedback components.
Available internal voltage options:

- 0.6 V
- 0.9 V
- 1.1 V
- 1.8 V
- 2.5 V
- 3.3 V

5.2.2. External Voltage Selection

The Output Voltage can be selected with the help of the external resistor divider according to the equation below:

$$R_{LFB} = \frac{0.6 \cdot R_{HFB}}{V_{OUT} - 0.6} \tag{3}$$

R_{HFB} - connected between V_{OUT} and FB nodes. Typical value is 200kΩ 1%
R_{LFB} - connected between FB and GND nodes.
Please see Table 5.1. below for selection the typical output voltage values:

Table 5.1. V_{OUT} Selection. External method

Output Voltage (V)	R_{HFB} (kΩ)	R_{LFB}(kΩ)
1.0	200.0	301.0
1.2	200.0	200.0
1.5	200.0	133.0
1.8	200.0	100.0
2.5	200.0	63.2
3.3	200.0	44.2

5.3. Selecting the Inductor

Determining the inductance is a key aspect of designing a buck converter. The equation below is the most common way to calculate an inductance:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{SW} \cdot \Delta I_L} \tag{4}$$

$\Delta I_L -$ is the inductor current ripple. The inductor current is chosen at approximately 30% of the maximum load current.
$f_{SW} -$ is the buck converter switching frequency

The peak current of the inductor, which affects its saturation, is also determined. The following equation shows how to calculate the peak inductor current:

$$I_{Lpeak} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{5}$$

5.4. Selecting the Output Capacitor

The output capacitor plays a crucial role in reducing the output voltage ripple, ensuring the stability of the feedback loop, and minimizing both overshoots and undershoots of the output voltage during load transients. To achieve the best performance, an output capacitor with large capacitance and low ESR is recommended. For most applications, a ceramic capacitor with a value between 10μF and 22μF is sufficient.

Important: Always check the DC bias voltage curve for your output capacitors to ensure they will perform as expected across the operating range.

5.5. Selecting Input Capacitor

The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Generally, 10μF or 22uF input capacitors are sufficient for most applications. Additionally, larger sizes result in higher parasitic inductance, which has a negative impact, but they offer improvements in electrical parameters such as capacitance and voltage rating.

5.6. Selecting Feed Forward Capacitor

A common method to improve the stability and bandwidth of a power supply is to use a feedforward capacitor, which is a capacitor placed across the high-side feedback resistor. We recommend using 33pF as a feed-forward capacitor.

5.7. Recommended Component Selection

Table 5.2. Recommended Component Selection

Output Voltage (V)	R_{HFB} (kΩ)	R_{LFB}(kΩ)	C_{IN} (μF)	C_{OUT} (μF)	L (nH)	C_{FF} (pF)
0.6	200	--	10+0.1	22	470	33
0.9	200	400	10+0.1	22	470	33
1.1	200	240	10+0.1	22	470	33
1.8	200	100	10+0.1	22	470	33
2.5	200	63.2	10+0.1	22	470	33
3.3	200	44.4	10+0.1	22	470	33

Note 3. **Resistor Accuracy:** The feedback resistors should be chosen with a minimum accuracy of 1%.
Note 4. Choose the input and output capacitors with a voltage rating that is 20% higher than the maximum V_{IN} and V_{OUT} voltage values. The capacitor size and temperature coefficient depend on the application and should be selected accordingly.
Note 5. If the internal voltage divider is selected, the FB pin should be left floating.

Table 5.3. List of components

Reference	Description	Manufacturer
IC	AM32103	Atlas Magnetics
L	74479275147	Würth Elektronik
C_{IN1}	885012105020	Würth Elektronik
C_{IN2}	885012205018	Würth Elektronik
C_{OUT}	885012107011	Würth Elektronik
C_{FF}	885012005010	Würth Elektronik
R1	Depending on V_{OUT}	Any
R2	Depending on V_{OUT}	Any
R3	100kΩ	Any

6. Recommended PCB Layout

6.1. Layout Guidelines

An efficient PCB layout of the switching power supplies is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues

1. Place the input capacitors as closely across V_{IN} and GND as possible. This is the most crucial placement of the components.
2. Place the output capacitors as closely across V_{OUT} and GND as possible.
3. Place the feedback components as close to FB as possible.
4. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance and reduce EMI.
5. Use multiple vias to link the internal PGND planes with the PGND plane on the top layer

6.2. Layout Example

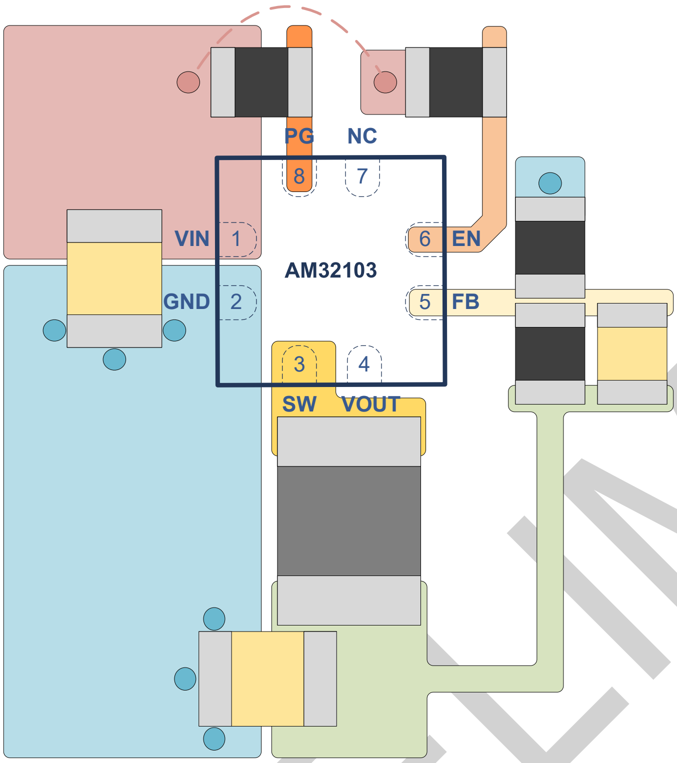


Figure 6-1. Recommended PCB Layout
(External Feedback)

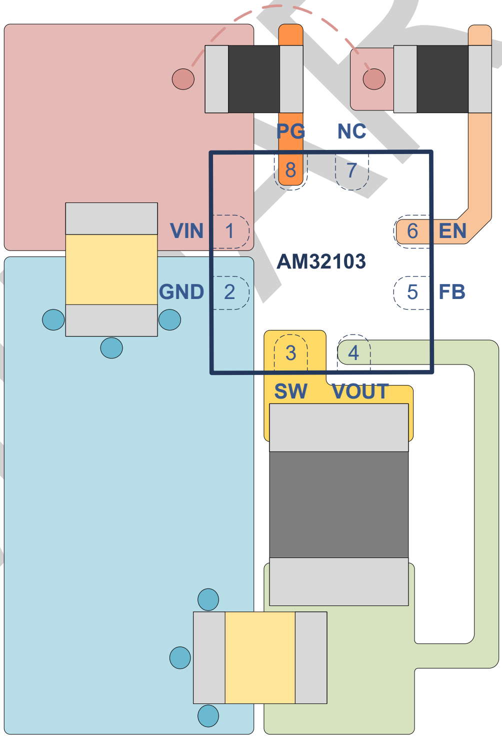
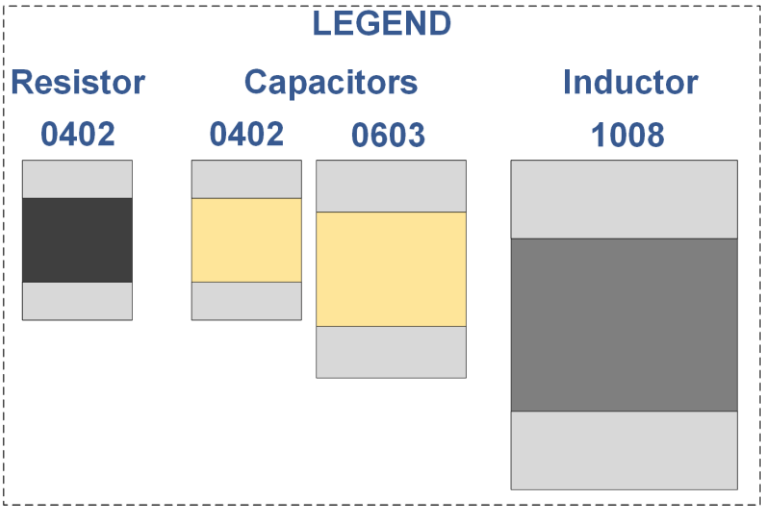


Figure 6-2. Recommended PCB Layout
(Internal Feedback)



6.3. Layout Stack-Up Proposal

A well-designed PCB layer stack-up is critical for DC-DC converters. It ensures low impedance power and ground paths, minimizes EMI, improves thermal performance, and supports reliable high-frequency switching operation. Proper stack-up design directly impacts efficiency, noise performance, and overall system stability. Please check our proposal below:

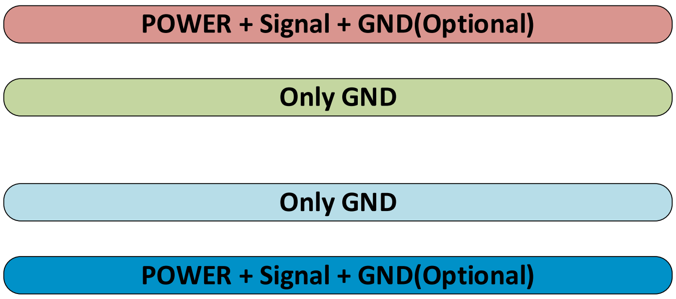


Figure 6-3. Layer stack-up of a four-layer board (Better for EMI performance)

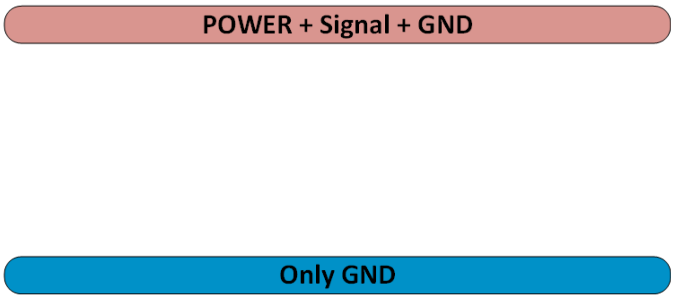
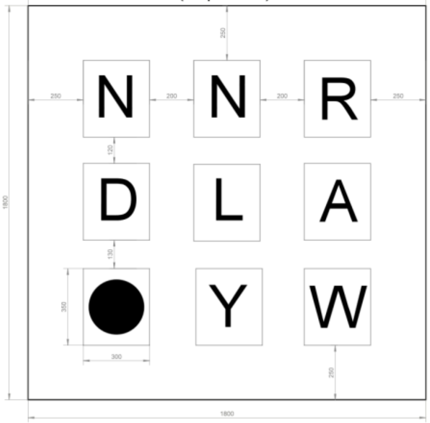


Figure 6-4. Layer stack-up of a two-layer board

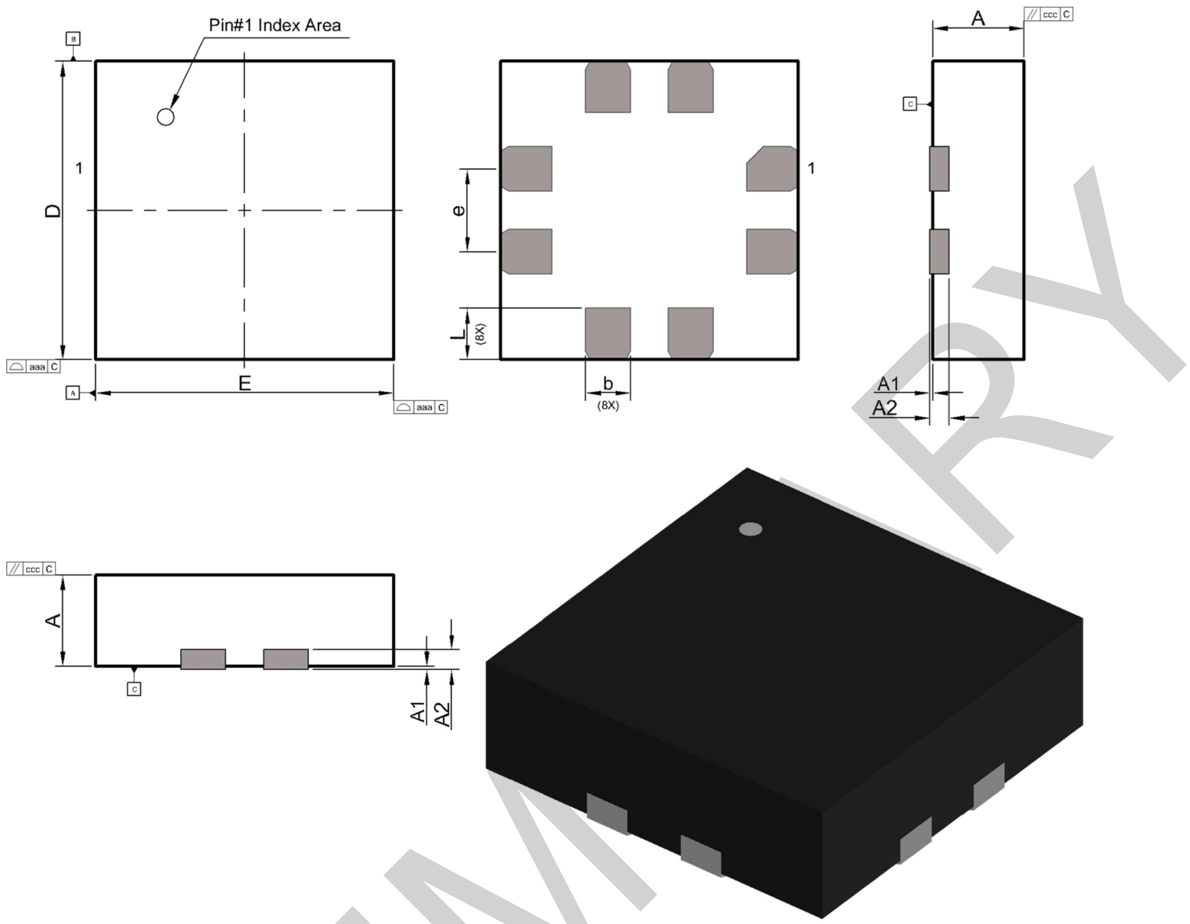
7. Package Top Marking System Definition

(Top View)



NN - Identification Code
R - Project Revision
D - Die Version
L - Wafer Lot ID
A - Assembly site ID
Y - Assembly Year
W - Assembly Week

8. Package Drawing and Dimensions



TQFN-8							
Symbol	**Min.**	**Typ.**	**Max.**	**Symbol**	**Min.**	**Typ.**	**Max.**
A	0.500	0.550	0.600	**L**	0.260	0.310	0.36
A1	0.005	0.020	0.030	**b**	0.220	0.270	0.320
A2	0.140	0.165	0.190	**e**	—	0.500	—
D	1.750	1.800	1.850	**aaa**	—	0.050	—
E	1.750	1.800	1.850	**ccc**	—	0.050	—
All Dimensions in mm							

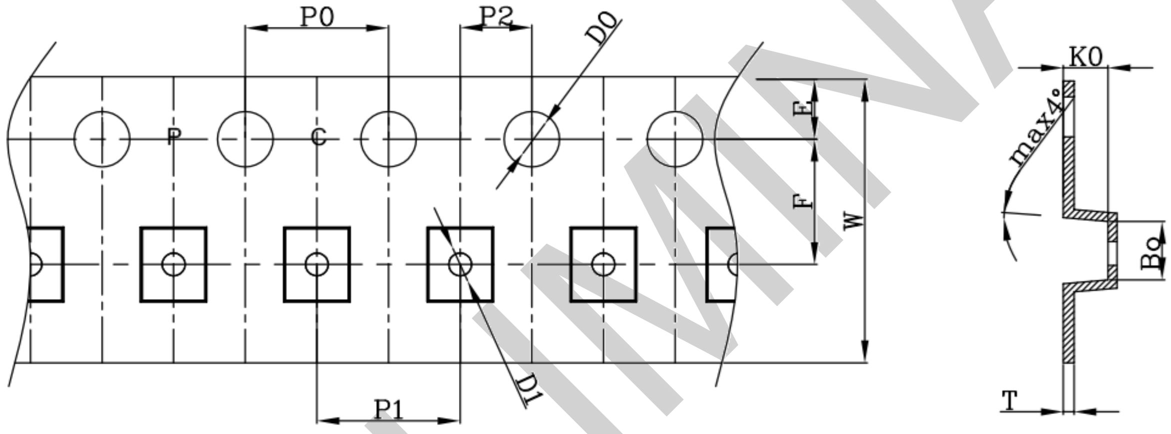
9. Tape and Reel Specifications

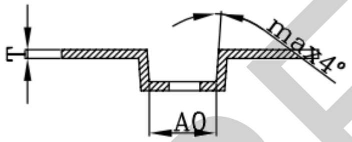
Table 9.1. Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size, mm	Max Units		per Reel & Hub Size, mm	Leader (min)		Trailer (min)		Tape Width, mm	Part Pitch, mm
			per Reel	per Box		Pockets	Length, mm	Pockets	Length, mm		
TQFN **Error! Unknown document property name.**L 0.5P FC	8	1.8× 1.8× 0.55	3000	3000	178/55	130	520	130	520	8	4

Table 9.2. Carrier Tape Drawing and Dimensions

Package Type	A0	B0	K0	P0	P1	P2	T	E	F	D0	D1	W
QFN1818-8	2.00	2.00	0.75	4.00	4.00	2.00	0.20	1.75	3.50	1.50	0.80	8.00





NOTE：
1. material: PC
2. 10 sprocket hole pitch cumulative tolerance +-0.2;
3. camber not to exceed 1mm in 250mm;
4. all dimension should met the requirements of EIA-481-D

10. Recommended Land Pattern

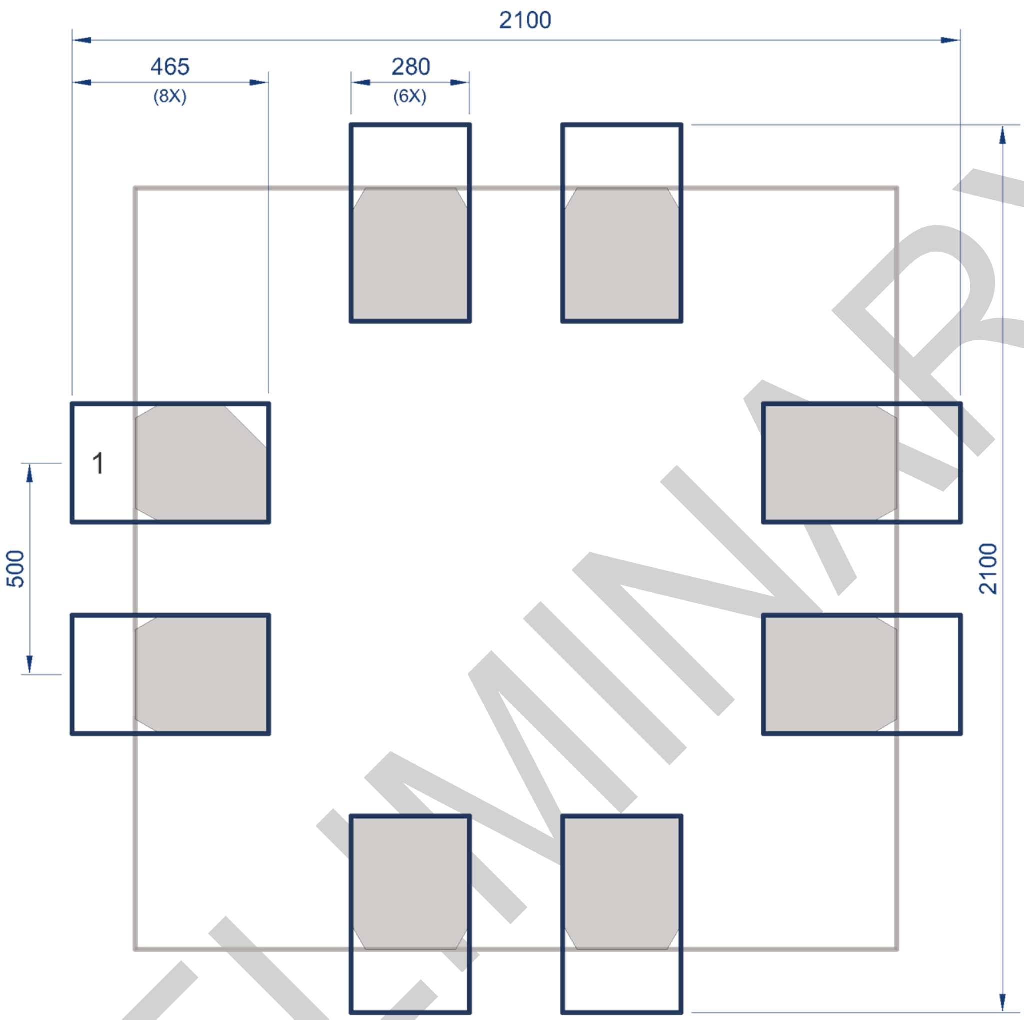


Figure 10-1. Recommended Land Pattern (Top View). Unit: µm

11. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.504 mm^3 (nominal). More information can be found at www.jedec.org.

12. Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Weight: 0.005008 grams (Approximate)

13. Revision History

Date	Version	Changes
3/11/2026	Rev.001	Initial release
3/30/2026	Rev. 002	Add Thermal resistance results

14. Worldwide Sales and Customer Support

Atlas Magnetics has established a vast network of offices, partners, distributors, and manufacturer's representatives. Feel free to contact any of the listed contacts to get in touch with us.

WEB support:
atlasmagnetics.com/contact

AM direct contacts:

Americas:	Taiwan, China, South Eastern Asia:	EMEA:
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