



ATLAS MAGNETICS

POWER SEQUENCER

Using μASIC

Abstract

This application note describes the proper timing of power rails within a system. The sequence and dependencies of power rails, along with the conditions for their activation and shutdown, are critical to system functionality and can vary significantly between designs.

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1. Power Sequencer Overview

1.1. Importance of Power Sequencer

A Power Sequencer is an essential component in electronic circuits, especially in systems with multiple power rails that require precise timing and order. It controls the activation and shutdown of voltage rails in a predefined sequence, preventing potential damage, minimizing inrush currents, and ensuring system stability. The key goal of the power sequencer is:

1. **Protecting Sensitive Components:** many modern electronic devices, such as FPGAs, microprocessors, and ASICs, require specific power-up and power-down sequences. If these sequences are not followed, components may malfunction or even sustain permanent damage due to excessive voltage stress or unintended current paths.
2. **Preventing Inrush Current Issues:** when multiple power rails turn on simultaneously, large inrush currents can occur, potentially:
 - a. Overloading power supplies
 - b. Triggering protection circuits
 - c. Causing voltage dips that affect system stability

By sequencing power rails properly, the current demand is distributed over time, reducing stress on the power supply and improving system reliability.

3. **Ensuring Proper Initialization of Components:** many integrated circuits (ICs) require core voltages (e.g., 1.2V) to be active before I/O voltages (e.g., 3.3V). If the I/O voltage is applied first, the IC might enter an undefined state, leading to erratic behavior or failure. Proper sequencing guarantees that each component starts up correctly.
4. **Avoiding Reverse Bias and Latch-up Conditions:** improper power-up sequencing can result in:
 - a. Latch-up conditions, where excessive current flows due to unintended parasitic transistors in ICs.
 - b. Reverse biasing of components, which can lead to electrical overstress and failure.

Power sequencing helps prevent these dangerous conditions by ensuring controlled voltage application.

5. **Enhancing System Reliability and Longevity:** by preventing stress on components and ensuring a smooth power transition, power sequencing extends the lifespan of electronic systems. It also reduces failures due to electrical stress, leading to higher reliability in mission-critical applications such as automotive, aerospace, and medical electronics.
6. **Compliance with Manufacturer Requirements:** Many semiconductor manufacturers specify power sequencing requirements in their datasheets. Failure to follow these guidelines can lead to warranty voiding or unstable operation. Proper sequencing ensures compliance with these requirements and maximizes system performance.

To better understand the importance of a power sequencer, let's consider a real-world example of its application. In this example, we have an MCU-based system with an additional sensor, powered by a DC/DC converter and an LDO (Low Dropout Regulator). The proper sequencing of power delivery is essential to ensure that the MCU and sensor are powered on/off properly.

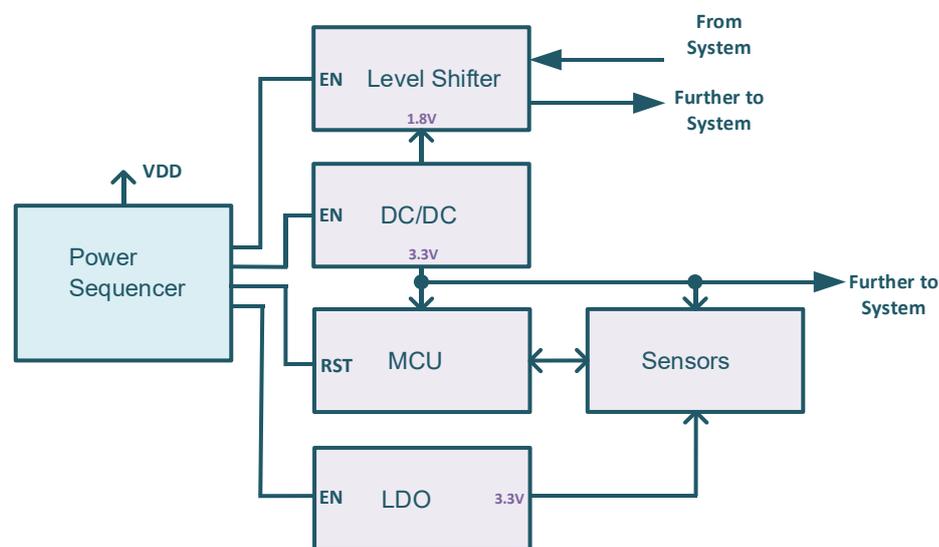


Figure 1.1. Power sequencer application example for MCU based system

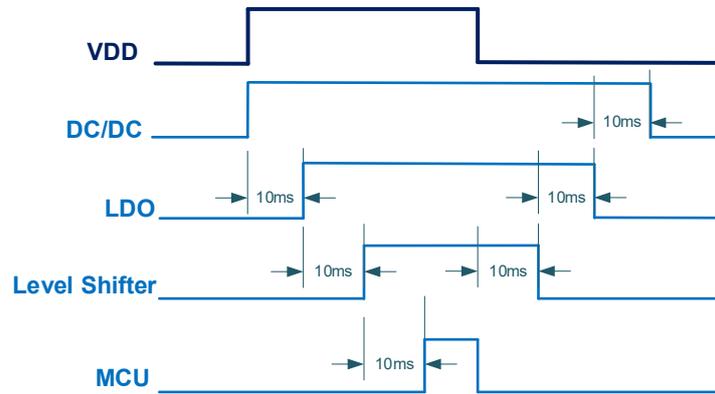


Figure 1.2. Power sequencer timing diagram example

1.2. Types of Power Sequencers

Power sequencers come in different types, each designed to handle specific applications based on complexity, power requirements, and system design. Below are the main types of power sequencer.

1.2.1. Time-Delay Power Sequencers

These sequencers operate on a time-based principle, introducing a delay between each power-up or power-down event. Each device in the system follows a preset delay, ensuring components stabilize before the next one is activated or deactivated. Time-delay power sequencers are widely used in audio systems to prevent speaker "thumps" and voltage spikes. This approach is also the simplest and most straightforward method for managing power distribution.

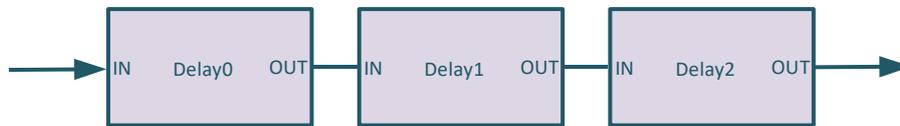


Figure 1.3. Time-Delay Power Sequencer

1.2.2. Voltage Monitoring Power Sequencers

These sequencers monitor the incoming voltage level and ensure that it reaches a specified threshold before allowing the next component to be powered up. This prevents devices from being powered on in the case of low or unstable voltage, protecting them from potential damage. Voltage monitoring power sequencers are commonly used in sensitive electronic systems where voltage fluctuations can cause harm or when the power supply is weak and cannot handle the simultaneous power-up of all components.

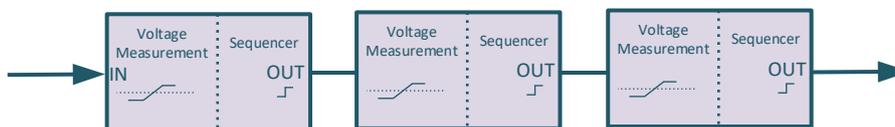


Figure 1.4. Voltage Monitoring Power Sequence

1.2.3. Current Sensing Power Sequencers

These sequencers monitor the current flow to each component and ensure that the drawn current remains within safe limits before allowing subsequent components to be powered up. Current-sensing power sequencers are commonly used in systems where the power supply has limited capacity and inrush current needs to be controlled, such as in data centers or laboratories, to prevent overloading the power source.

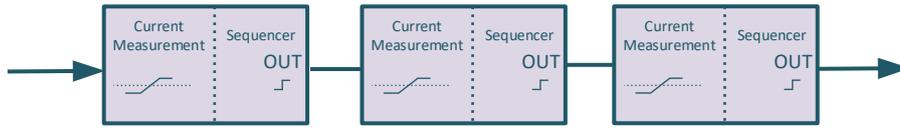


Figure 1.5. Current Sensing Power Sequencer

1.2.4. Programmable Power Sequencers

These sequencers provide the flexibility to customize power sequencing patterns. Users can define the exact sequence, timing, voltage, and current levels for individual components or groups, ensuring precise control over the power-up and power-down process. Programmable power sequencers are widely used in complex electronic systems where components have specific requirements and dependencies. They can be implemented using an MCU, FPGA, or a configurable mixed-signal IC like μ ASIC.

1.3. Power Sequencers Implementation Approaches

The implementation of a power sequencer can be approached in several ways, depending on the application requirements, complexity, and available resources. Here are some common approaches to implementing power sequencers.

1.3.1. Discrete Component-Based Implementation

Description: Discrete-component-based power sequencers utilize elements such as resistors, capacitors (often forming RC circuits for time delay), diodes, transistors, digital gates, flip-flops, and other discrete components to implement sequencing logic.

Use Case: Suitable for simple applications where basic control is required.

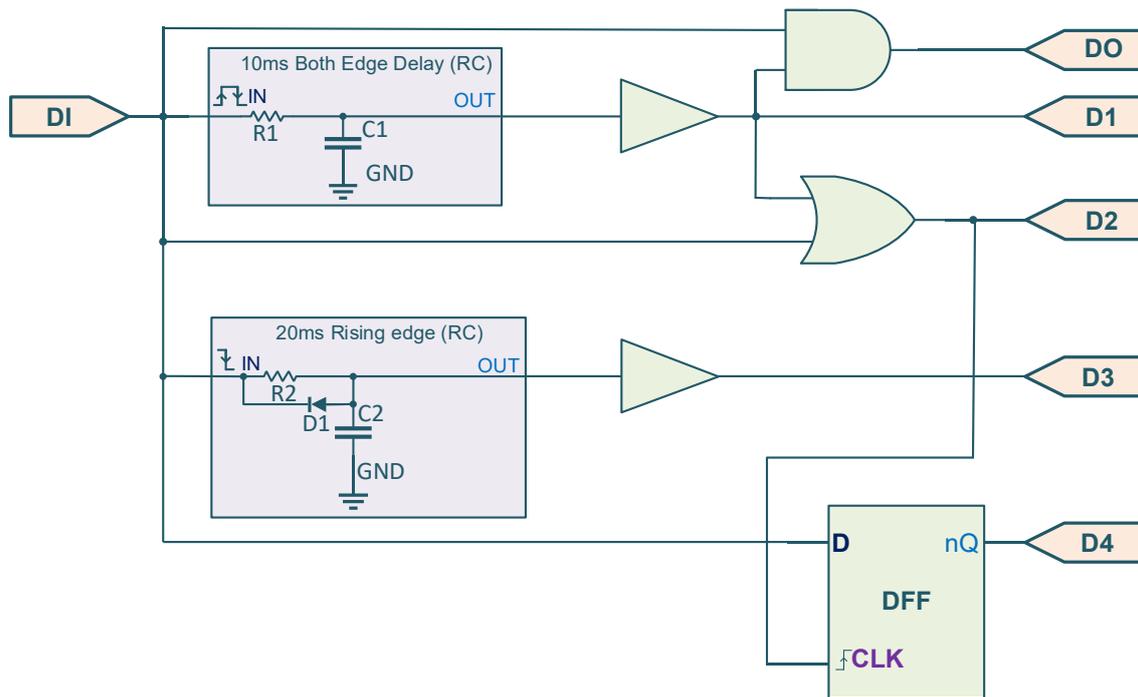
Advantages: Relatively low cost.

Disadvantages: Limited flexibility, lack of programmability, complex design for advanced power sequencing, and larger PCB space requirements. Additionally, they may not provide precise timing and control for complex systems.

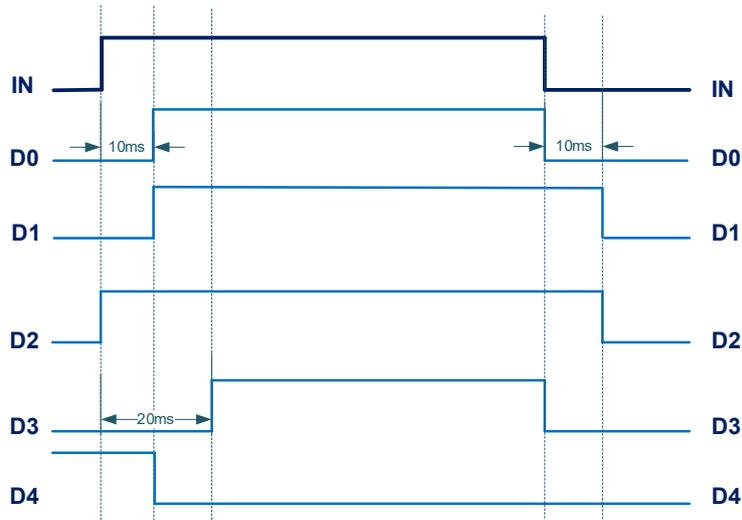
Additional Considerations: Discrete power sequencers typically consume less power than microcontroller-based solutions but can still draw tens of microamps in standby mode. When choosing a discrete sequencing solution, the designer must consider at least one of the following trade-offs:

- **Fixed sequencing:** If the implementation has fixed sequencing, the designer must choose an IC with timing delays longer than the optimal sequencing times, requiring system adjustments to match the selected power sequencer IC.
- **Externally configurable with passives:** If the implementation allows external configuration using passive components, the total solution size will be larger.
- **Programmable discrete implementation:** If the implementation is programmable, it will result in higher cost and increased current consumption.

One of possible variants for discrete solutions can be found below on [Figure 1.6 \(a\)](#).



a)



b)

Figure 1.6. Power sequencer example

1.3.2. Microcontroller (MCU) Based Implementation

Description: An MCU can be programmed to control the sequencing of power to different components based on user-defined parameters. The MCU approach gives the greatest flexibility over the entire power tree since firmware easily defines many inter-dependent states.

Use Case: Common in embedded systems and applications where custom logic is needed.

Advantages: High flexibility, ability to adapt to changes, and easier integration with other digital systems.

Disadvantages: Higher cost, increased system complexity, relatively slow reaction/long latency, higher current consumption, reliability.

Additional Considerations:



- **Latency:** As synchronous systems, microcontrollers prioritize power efficiency at the expense of reaction time. In a power sequencer, this trade-off can limit the ability to respond quickly to faulty conditions. Additionally, the minimum clock speed imposes a baseline power consumption for the device.
- **Reliability:** Power sequencing is controlled by firmware rather than hardware. However, using firmware introduces potential risks, as it creates a dependency between the power sequencing process and any additional code being executed. Firmware updates or unintended bugs—even those unrelated to power sequencing—can inadvertently impact the power rail. Since power sequences, like resets and watchdog timers, are critical “must-not-fail” functions, any errors could have severe consequences, potentially leading to system failure or permanent device damage.

1.3.3. Field-Programmable Gate Array (FPGA) Based Implementation

Description: FPGAs can be used to create custom logic for power sequencing, providing real-time control and monitoring capabilities.

Use Case: Ideal for high-performance applications that require complex power management, such as telecommunications and high-speed computing.

Advantages: Highly customizable, capable of handling multiple components and complex dependencies.

Disadvantages: High cost and complexity; require expertise in digital design.

1.3.4. Configurable Mixed-Signal ICs (μ ASIC) Based Implementation

Description: Configurable Mixed-Signal ICs are a specialized class of integrated circuits that blend flexibility with high performance. They enable the design of various power sequencers, providing extensive timing and voltage adjustability while ensuring adaptability to different system requirements.

Use Case: Ideal for any type of power sequencer implementation.

Advantages: High flexibility, ability to adapt to changes, easy integration with other analog and digital systems, high reliability, low power consumption, low latency, small footprint (no external component is needed), low cost, simple and efficient configuration.

Disadvantages: -



2. Power Sequencer Based on μ ASIC

The configurable μ ASIC is perfect for power sequencing, eliminating the need to compromise between low latency, low power, configurability, and board size. Using the free Atlas EDA software, engineers can easily set up custom timing profiles, monitor specific voltages, configure logic and behavior, debug the device independently, and receive samples within 2 to 3 weeks.

2.1. Power Sequencer (AM1U1108)

Let's take as an example circuit from Figure 1.6 (a). It is a simple sequencer but if to look on timing diagram from Figure 1.6 (b) we can see that power ON differ from power OFF sequence, it is not symmetrical power sequencer, also after D4 is LOW it is latched and remain in such state regardless of input. So, it is custom type sequencer, specialized for unique proprietary system.

Note: This example uses the AM1U1108 part, an 8-pin μ ASIC with 1.0mm x 1.2mm package size.

To achieve the same result as shown in Figure 1.6 (a) on μ ASIC, the design requires several LUTs, timers, and a DFF cell to latch the D4 signal (see Figure 2.1). The configuration of the μ ASIC part is easily doable in Atlas EDA software. The advantage of this approach is its flexibility, timing and sequence order can be adjusted by simple update of the configuration, allowing for a configuration that precisely matches system's requirements.

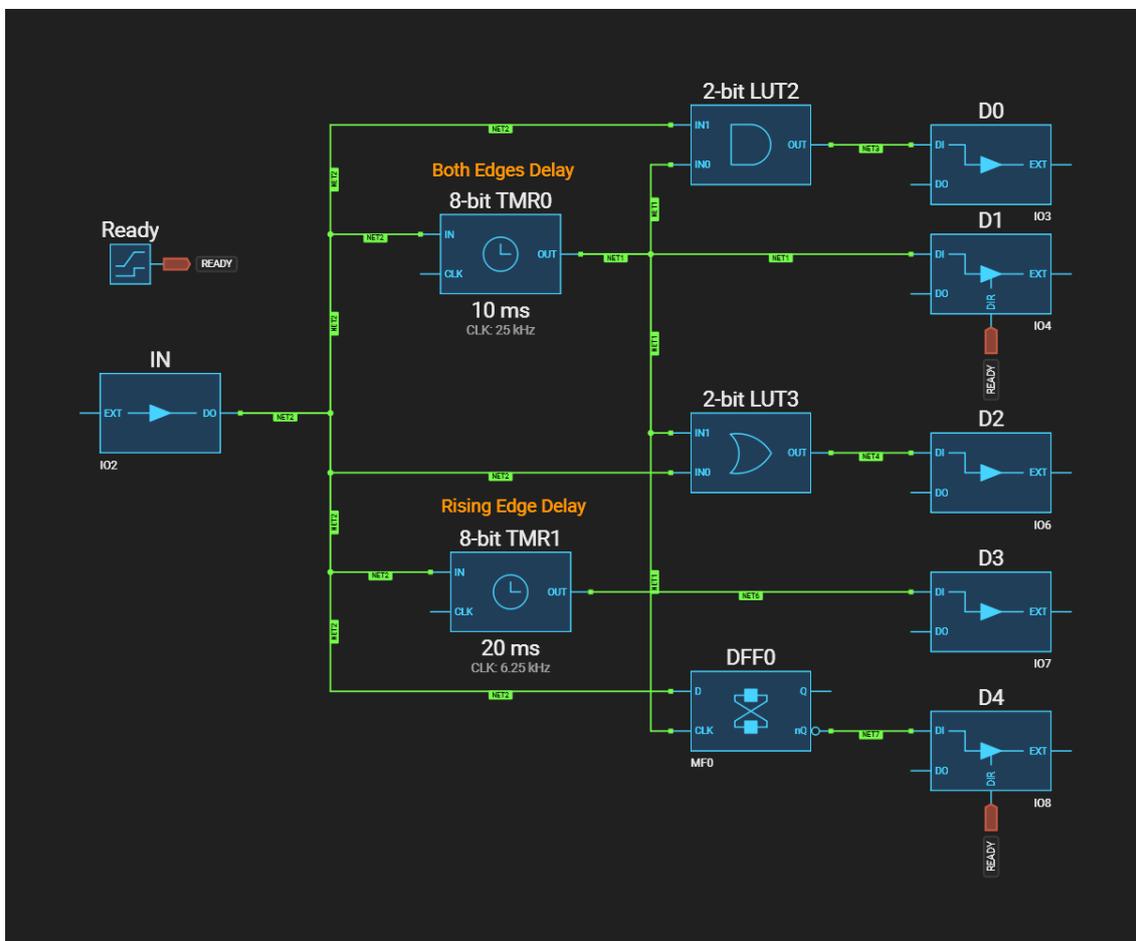


Figure 2.1. Power sequencer design (AM1U1108)

Signal Flow:

1. IO2 ("IN") LOW to HIGH Transition:

- D0 goes high 10ms after IN (IO2) input goes high. It is defined by the 10ms delay generated based on the TMR0, and once the 10ms delay expires the output goes high as both input of AND gate (LUT2) is high.
- D1 goes high 10ms after IN (IO2) input goes high. It is defined by the 10ms delay generated based on the TMR0.



- **D2** goes high immediately after IN (IO2) input goes high. It is defined by OR gate (2-bit LUT3), which has input directly from IN and Both-edge timer.
- **D3** goes high 20ms after IN (IO2) goes high. It is defined by the 20ms delay generated based on the TMR1.
- **D4** goes low 10ms after IN (IO2) goes high. It depends on the DFF0. Clock input takes signal from TMR0 and D input from IN (IO2), so the IN (IO2) value will be triggered to DFF0 once the TMR0 completes 10ms delay.

2. IO2 ("IN") HIGH to LOW Transition:

- **D0** goes low simultaneously with IN (IO2), as the signal instantaneously propagates through the AND (LUT2) gate to the D0 (IO3) output.
- **D1** goes low 10ms after IN (IO2) goes low. It depends on TMR0, once it completes 10ms delay.
- **D2** goes low 10ms after IN (IO2) goes low. It is formed by OR gate (2-bit LUT3) between IN and TMR0, so it will output low when both inputs are low, this generates 10ms delay on falling edge.
- **D3** goes low simultaneously with IN (IO2), as the TMR1 is configured as Rising edge delay and goes low immediately once the input is dropped low.
- **D4** remains Low because **DFF0** remains latched until the chip is reset.

This setup ensures a well-coordinated delay mechanism, controlling signal transitions with precise timing across different outputs, voltages and temperatures.

2.1.1. Bench Results

Below is a real-world test result, that proves the correctness of our design:

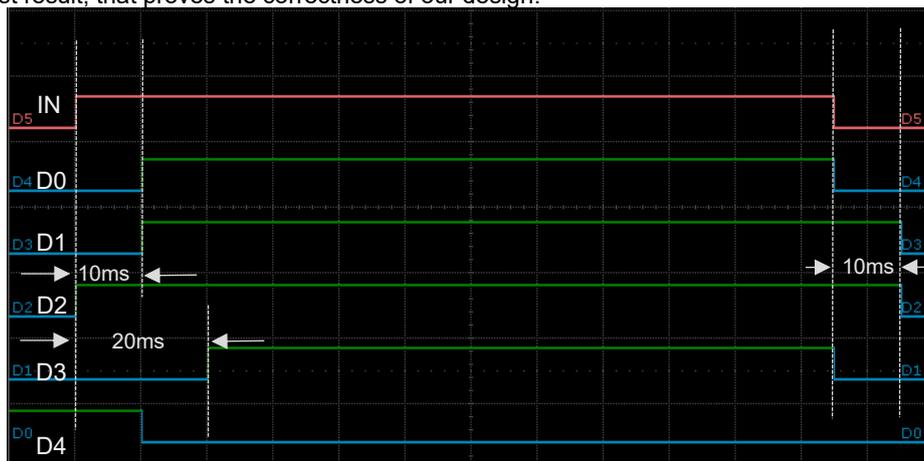


Figure 2.2. Real waveform from device.

2.2. Power Sequencer with analog input (AM1U1408)

The following example shows a power sequencer that controls lithium-ion battery management system based on voltage thresholds. It follows a symmetrical timing diagram, ensuring consistent behavior. To initiate the power-on sequence, the voltage at the analog input must exceed 3.3 V. Conversely, when the battery voltage drops below 3 V, the sequencer triggers the power-off sequence and system is turned off. This method helps regulate power management, preventing deep discharge and ensuring reliable operation.



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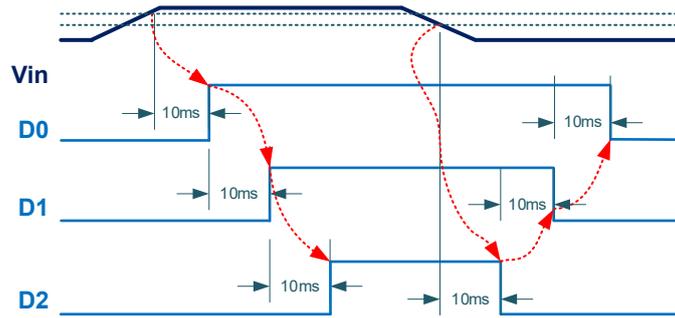


Figure 2.3. expected time diagram

Note: This example features the AM1U1408, one of the smallest mixed-signal IC — an 8-pin μ ASIC with a compact 1.0mm x 1.2mm package and an integrated ACMP.

To configure the μ ASIC part, Atlas EDA software was used. The design requires an ACMP (Analog Comparator), a timer (configured for Delay on Rising Edge), D-Flip-Flop, and LUTs with a custom configured truth table. The threshold voltages can be easily adjusted by modifying the VREF of the ACMP. The timing is easily adjustable with TMR0.

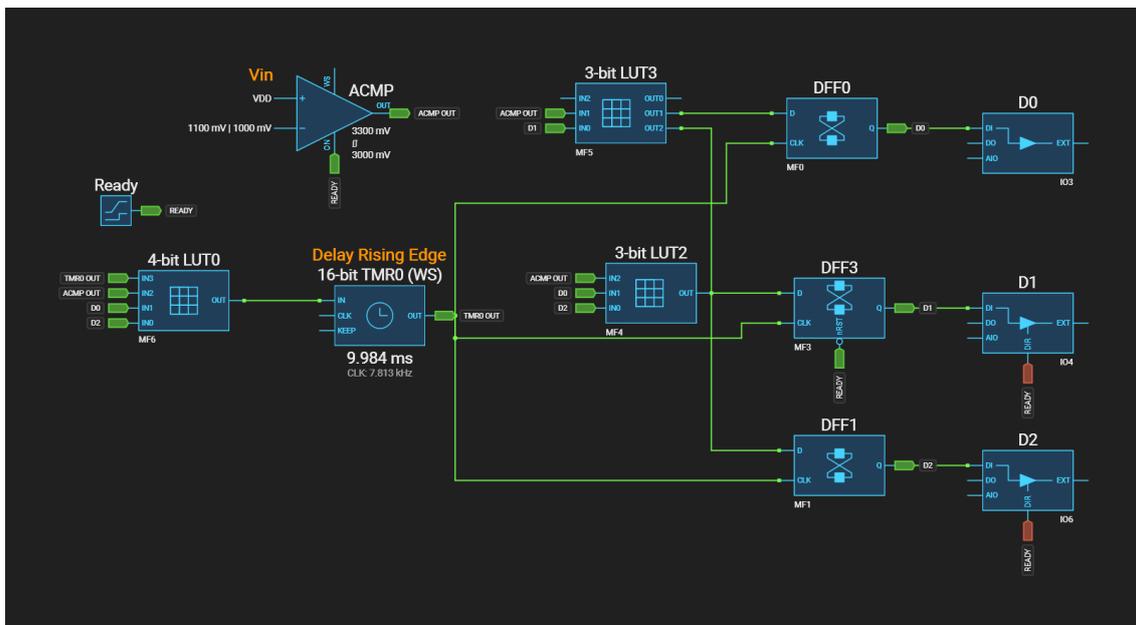


Figure 2.4. Power Sequencer (AM1U1408)



Table 1. Truth Table of 3-bit LUT3 (a) and 3-bit LUT2 (b)

IN0	IN0	IN1	OUT0	OUT1	OUT2
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	1

a)

IN0	IN1	IN2	OUT0
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

b)

Table 2. Truth Table of 4-bit LUT0.

IN0	IN1	IN2	IN3	OUT0
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	1	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

This schematic creates a symmetrical power sequencer that behaves next way:

- **D0** – goes high 10ms after voltage reaches 3300 mV.
- **D1** – goes high 10ms after **D0**.
- **D2** – goes high 10ms after **D1**.

And when the voltage on V_{in} drops less than 3V it will turn off:

- **D2** – goes Low 10ms after voltage drops to 3V (or less).
- **D1** – goes Low 10ms after **D2**.
- **D0** – goes Low 10ms after **D1**.

Let's look at how the design works.

When the voltage on **VDD (V_{in})** reaches 3300 mV, the **ACMP** output sets to logic 1. This signal is passed to **TMR0** through **4-bit LUT0**, which provides a 10 ms delay. After the delay, the **TMR0** output goes high, triggering the **CLK** input of **DFFs**, setting the first stage to 1. The **TMR0** signal then returns to **LUT0**, resetting **TMR0** and setting its output to 0, restarts, counts another 10 ms, and sets the second **DFF** to 1. This process continues, activating each **DFF** in sequence. Once all **DFFs** are set high the **TMR** stops counting.

When the voltage on **VDD** drops to 3000 mV, **ACMP** goes low, which activates the **4-bit LUT0**, and sequence goes in reverse.

- **LUT3** has three outputs, each with its own logic:
- **OUT0** is always 0 (inactive).
- **OUT1** functions as an OR gate, outputting HIGH if either **Q** from **DFF3** or the **ACMP** output is HIGH.
- **OUT2** functions as an AND gate, outputting HIGH only when both **Q** from **DFF3** and the **ACMP** output are HIGH.

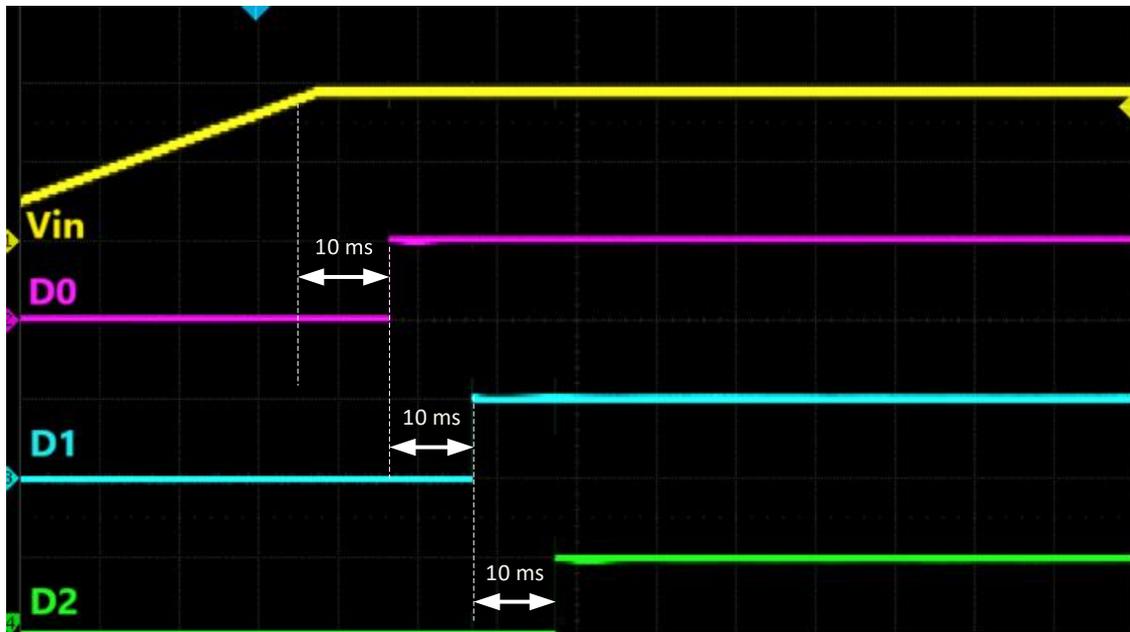
Another **3-bit LUT2** acts as a 2-to-1 multiplexer (MUX). The **ACMP** output (**IN2**) serves as the select input, choosing between **Q** from **DFF0** (**IN1**) or **Q** from **DFF1** (**IN0**).



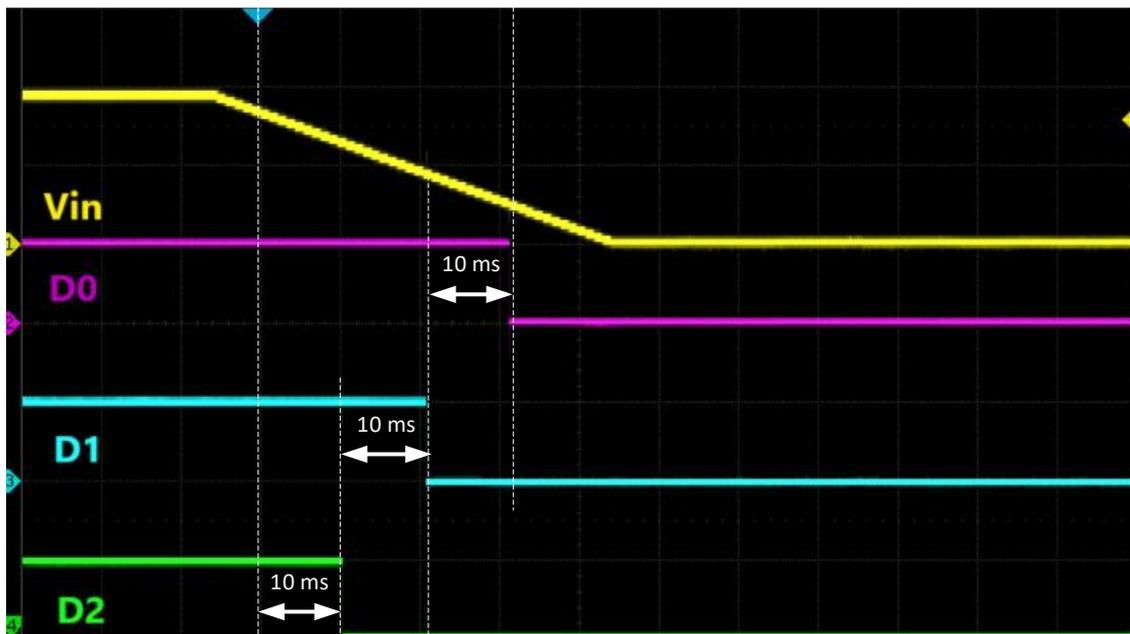
Oscillator is configured in auto on mode, what is reducing the chip power consumption to the minimum as OSC is turned ON only during the sequence up or down and is automatically turned OFF once the sequence is finished.

2.2.1. Bench result

Let's do some real-world testing and see if our expectations were proved by design:



a) Power On Sequence



b) Power OFF Sequence

Figure 2.5. Waveform of power sequencer

2.3. Power sequencer (AM1U1320)

This power sequencer example demonstrates handling multiple analog inputs and numerous outputs (Figure 2.6). To accommodate these requirements, μ ASIC with bigger IOs count is needed. This example uses the AM1U1320, a 20-pin μ ASIC.



Power Sequencer using μ ASIC

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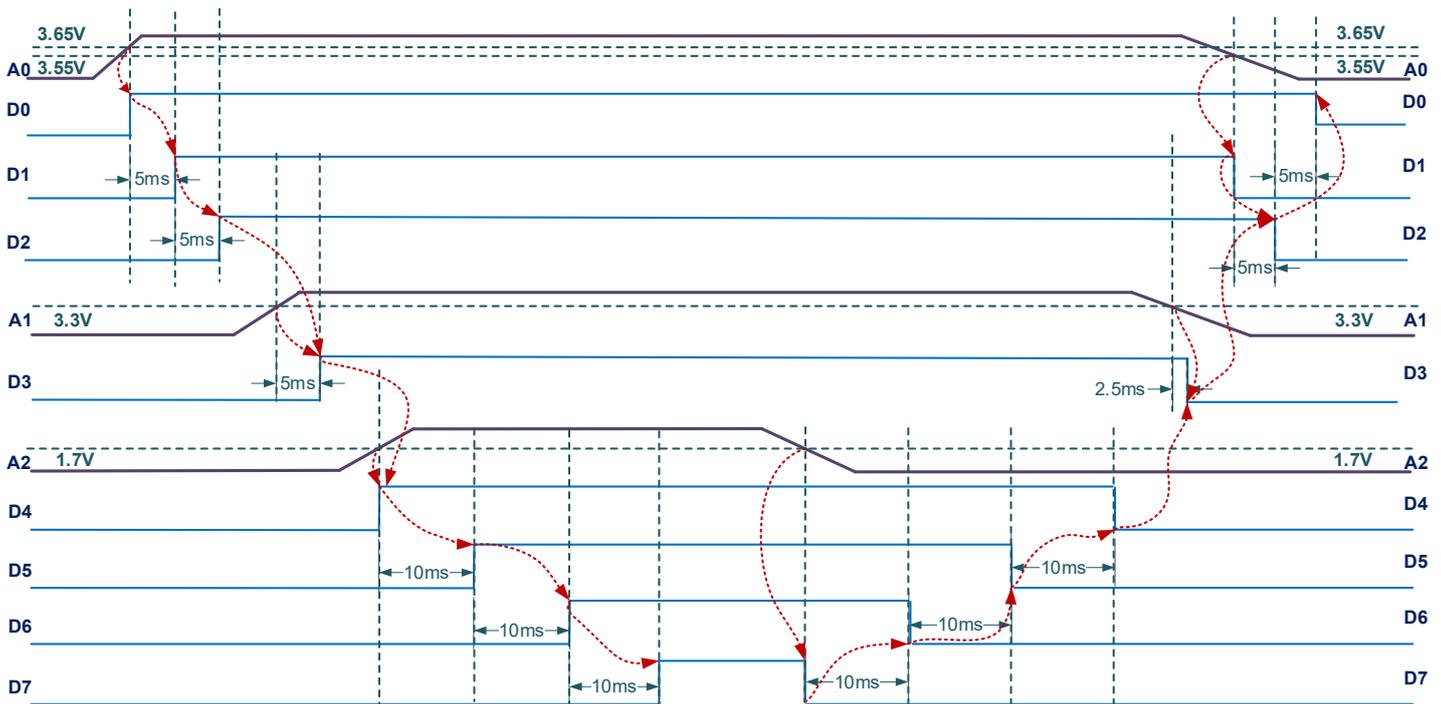


Figure 2.6. Power Sequencer Timing Diagram

For a clearer understanding of the design, refer to [Figure 2.7](#). The figure illustrates the power sequencer concept, which can be directly replicated to expand the sequencer for additional stages. This approach provides a universal method for creating a power sequencer.

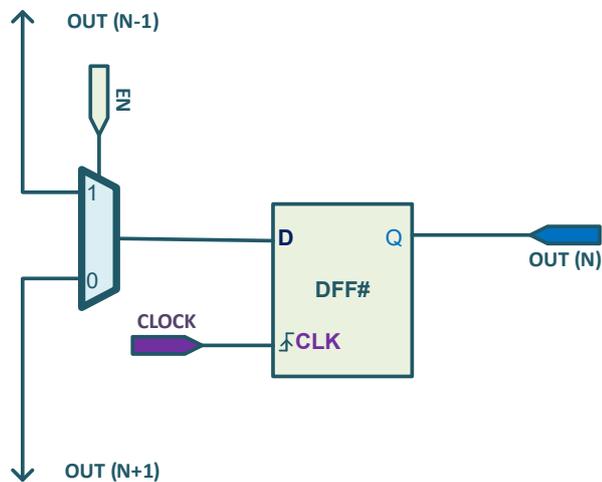


Figure 2.7. Concept of Power Sequencer.

In this concept, a 2:1 MUX is used to switch values based on the EN state (whether the system is on or off). Namely one signal is used during the power on and another signal during power off sequence.



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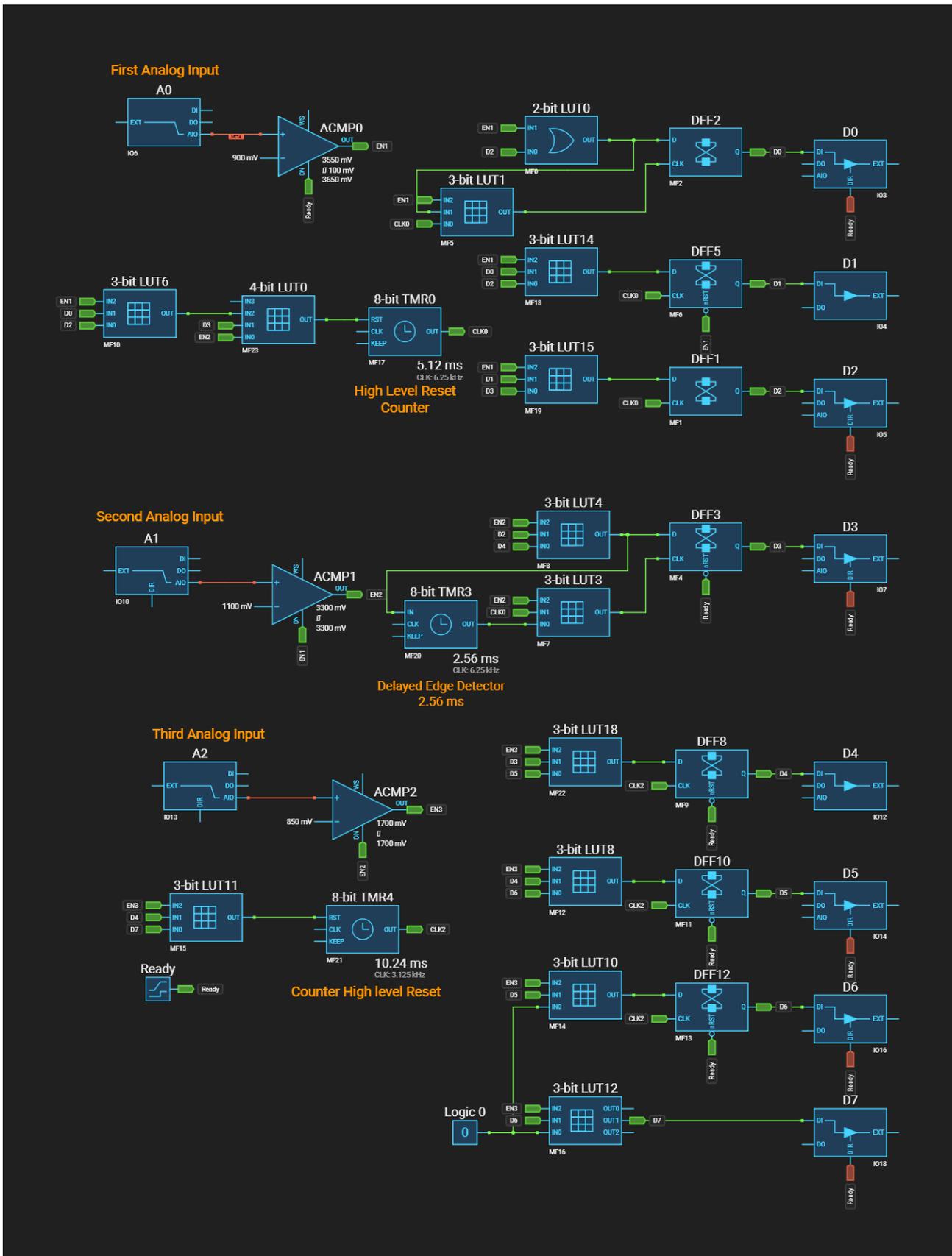


Figure 2.8. Design of Power sequencer (AM1U1320)

Let's look at each part of design for clearer understanding.



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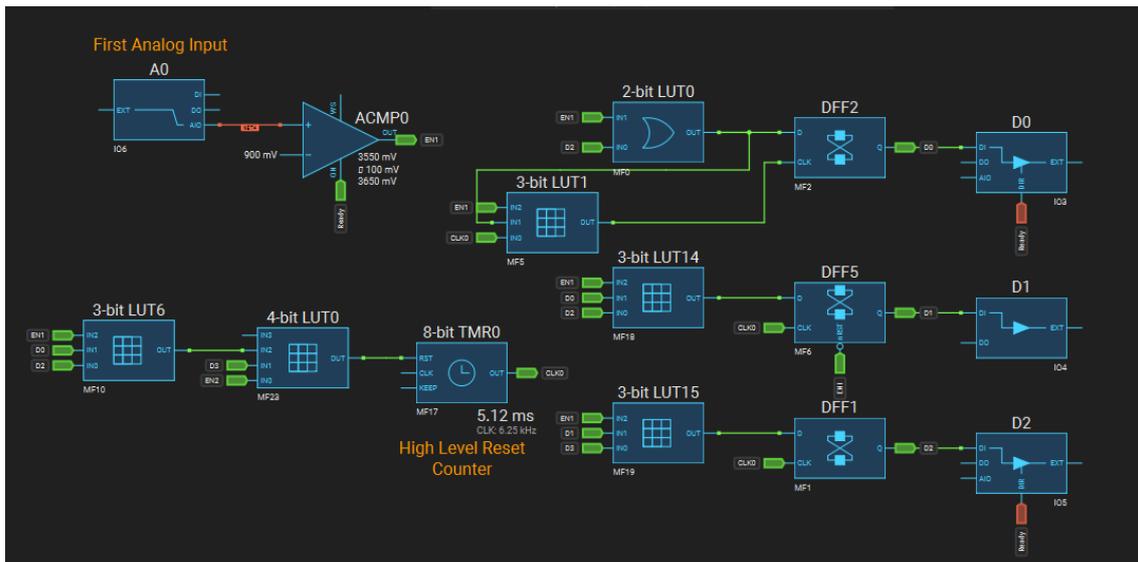


Figure 2.9. The First Part of Power Sequencer.

This section is controlled by an 8-bit TMR0 and ACMP0 that produces EN1 signal. EN1 is activated when the voltage at A0 (IO6) reaches 3650 mV, enabling the next ACMP and starting a sequence. Additionally, EN1 activates a timer configured as a Counter High-Level Reset. The sequence begins with D0 activating immediately, followed by D1 after 5.12 ms, and D2 after another 5.12 ms. Once all outputs are active, the 8-bit TMR0 is turned off to reduce power consumption.

When the voltage at A0 drops below 3550 mV, the system shuts down in reverse order. First, D1 turns off immediately and depends only on ACMP0, followed by D2 after 5.12 ms, and finally, D0 turns off after another 5.12 ms.

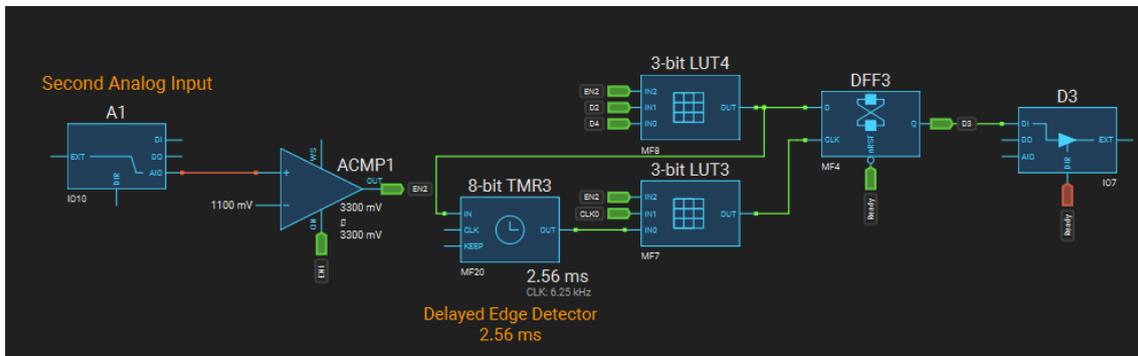


Figure 2.10. The second part of Power Sequencer

This second stage is controlled by EN2 (ACMP1), CLK0 (8-bit TMR0, as shown in Figure 2.9), and an 8-bit TMR3. EN2 is triggered when the voltage at A1 (IO10) reaches 3300 mV, activating the ACMP2. Upon receiving the EN2 signal, D3 is activated after a 5.12 ms delay. When the voltage at A1 drops below 3300 mV, the last ACMP is turned off, and D3 is deactivated after a 2.56 ms delay.

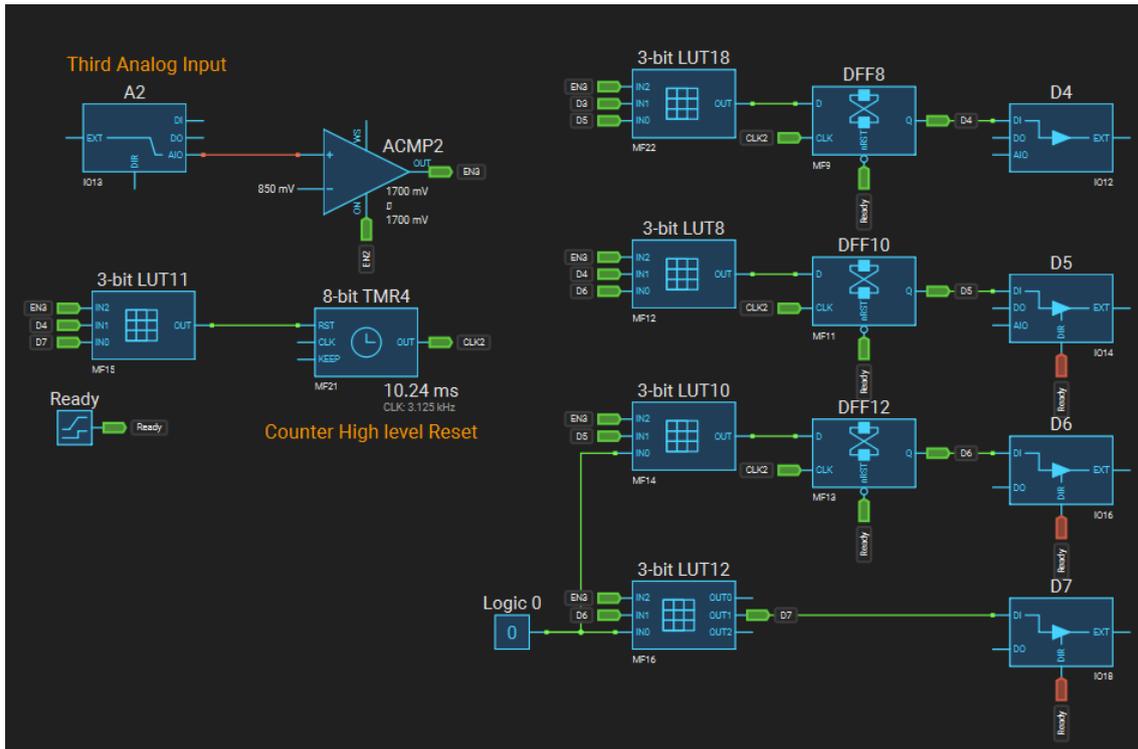


Figure 2.11. The Last Part of Power Sequencer

The final stage of the power sequencer is controlled by EN3 (ACMP2) and CLK2 (8-bit TMR4) signals, forming a symmetrical sequence except for the D7 and D4 outputs. D4 switches to logic 1 on the rising edge of EN2, while D7 immediately switches to logic 0 when the voltage at ACMP2 drops below the threshold.

Oscillator is configured in auto on mode, what is reducing the chip power consumption to the minimum as OSC is turned ON only during the sequence up or down and is automatically turned OFF once the sequence is finished.

2.3.1. Bench result

Let's check how design works in real life:

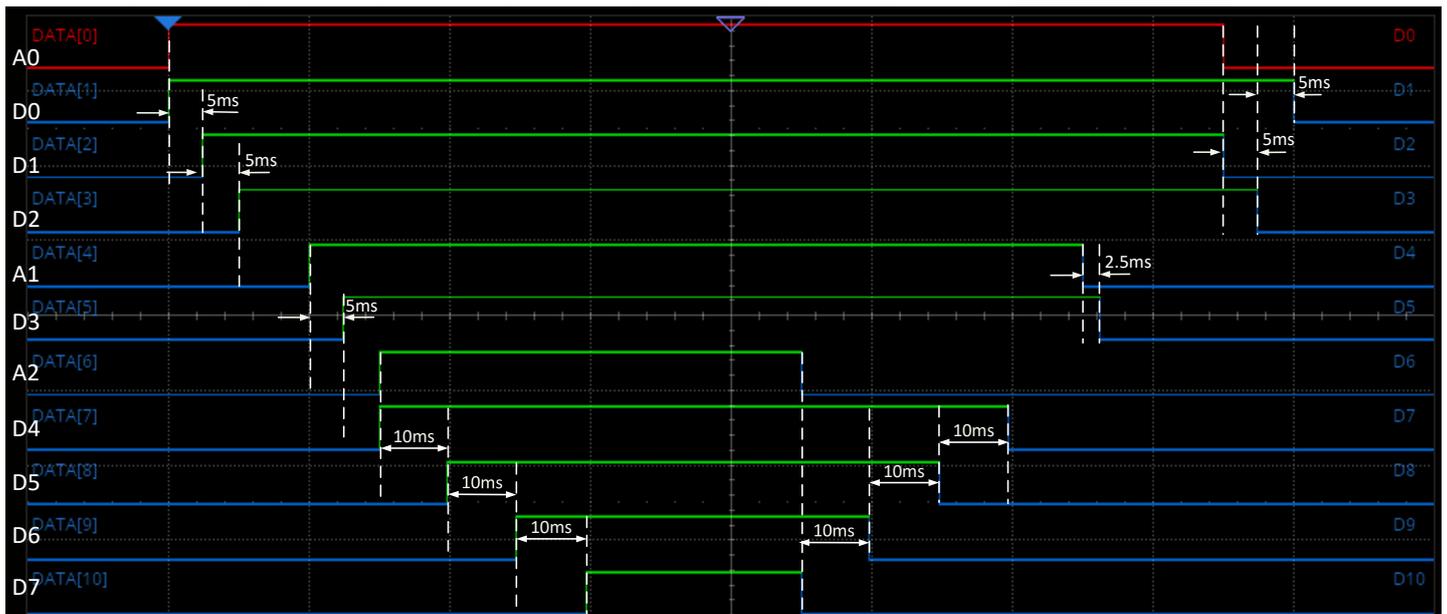


Figure 2.12. Waveform of Power Sequencer (AM1U1320).

The waveform of Power Sequencer completely repeats the power sequencer timing diagram (Figure 2.6).



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Summary

This application note has provided an understanding of power sequencer purpose, type and the critical role power sequencers play in ensuring reliable and efficient operation of modern electronics.

Additionally, this application note has explored various power sequencing techniques, including the use of discrete solution, dedicated power sequencer ICs, embedded microcontrollers, and configurable mixed-signal ICs. It has emphasized the benefits of configurable sequencers, allowing customization to meet different system requirements.

By leveraging the knowledge and guidelines presented here in this application note, designers can unlock the full potential of their configurable μ ASIC designs, enabling them to meet the demands of modern electronic systems with confidence.



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Want to Learn More About μ ASIC?

If you would like to learn more about this design or explore how it can be modified to perfectly fit your needs, we are here to help. Our team of experts is ready to provide you with valuable insights, technical expertise, and tailored solutions. Get in touch with us via email at crm@atlas-magnetics.com

To explore the latest updates and other valuable information, we invite you to visit our website at atlas-magnetics.com or check out our LinkedIn page [linkedin.com/company/atlas-magnetics](https://www.linkedin.com/company/atlas-magnetics).



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3. Revision History

Date	Version	Change
January 14, 2026	Rev.001	Initial release



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