AM1U1514

µASIC
Programmable Mixed-Signal IC

Description

The AM1U1514 is an ultra-small programmable µASIC featuring Logic Macrocells, Timers, Oscillators, ACMPs, Temperature Sensor, VREF and more. Each Macrocell within the AM1U1514 contains multiple, configurable settings and initial states for maximum flexibility.

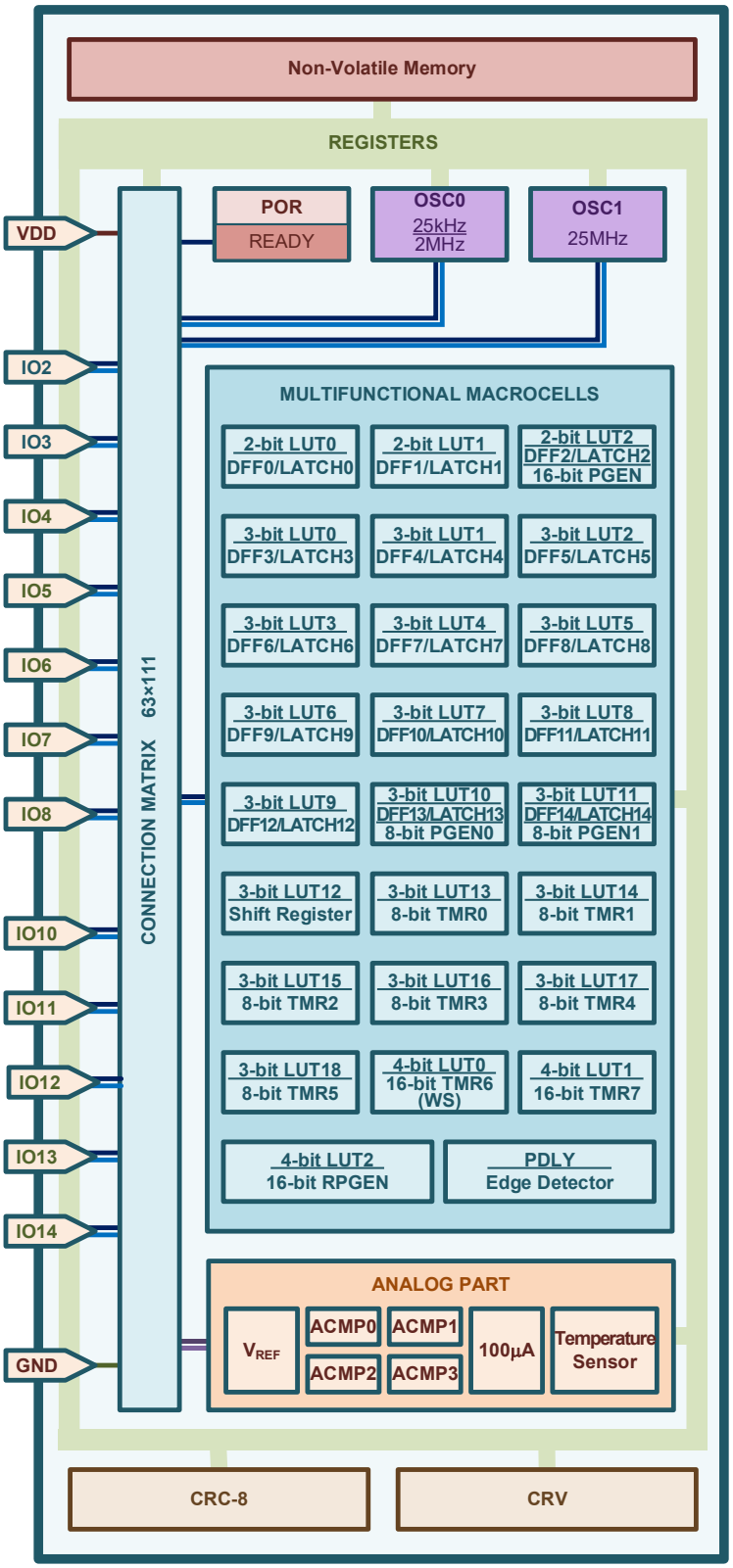
The AM1U1514 Macrocells are connected via hardware-defined matrix connections, not abstracted firmware. This enables asynchronous design at low power as well as more reliable operations compared to microcontrollers. Unlike a fixed ASIC, the timing and event sequences can be updated with a programming code change.

AM1U1514's functional reliability is enhanced by CRC-8 and Continuous Register Verification (CRV).

Features

- 1.71 V to 5.50 V Supply (V_{DD})
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant/Halogen-Free/Pb-Free
- Four Analog Comparators (ACMP)
- Voltage Reference (VREF)
- Temperature Sensor (TS)
- 100µA Current Source
- Twenty-Six Multifunctional Macrocells
  - Two Selectable 2-bit LUTs or DFF/LATCHs
  - One Selectable 2-bit LUT or DFF/LATCH or 16-bit Pattern Generator
  - Ten Selectable 3-bit LUTs or DFF/LATCHs
  - Two Selectable 3-bit LUTs or DFF/LATCH or 8-bit PGEN
  - One Selectable 3-bit LUT or 16-bit Shift Register
  - Six Selectable 3-bit LUTs or 8-bit Timers (TMR)
  - Two Selectable 4-bit LUTs or 16-bit Timers
  - One Selectable 4-bit LUT or 16-bit Reversible Pattern Generator
  - One Programmable Delay or Edge Detector
- Two Oscillators (OSC)
- Power On Reset (POR)
- Data Protection Feature
  - CRC-8
  - Continuous Registers Verification (CRV)
- Package Options
  - 14-pin TQFN (2.2×2.0×0.42 mm, 0.4 mm pitch)

Architecture Block Diagram



The AM1U1514 (Figure 1.1, Table 1) has 12 multi-function IO pins which can function as a user-defined Input or Output. Refer to Table 1 for pin definitions.
All of 12 user's-defined IO pins on the AM1U1514, pins can serve as Digital Input and Digital Output. IO2, IO3, IO5, IO6, IO7, IO8, IO10, IO11, and IO12 can also serve as Analog Input/Output.

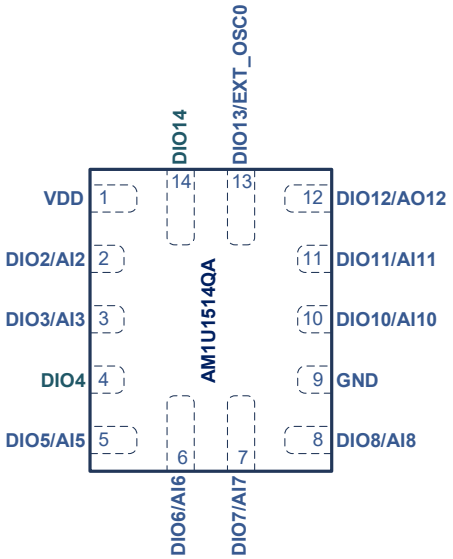


Figure 1.1. Top View (14-pin TQFN-A)

Table 1 Functional PIN Description

PIN # TQFN-14	PIN Name	Signal Name	Function	Input Options	Output Options
1	VDD	VDD	Power Supply	--	--
2	IO2	DIO4	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI2	Analog Comparator 1 Positive Input (ACMP1+)	Analog	Analog
3	IO3	DIO3	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI3	Analog Comparator 2 Positive Input (ACMP2+)	Analog	Analog
4	IO4	DIO4	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
5	IO5	DIO5	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI5	Analog Comparator 0 Positive Input (ACMP0+)	Analog	--
6	IO6	DIO6	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI6	VREF Input	Analog	--
7	IO7	DIO7	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AIO7	Analog Comparator 0 Positive Input (ACMP1+) 100µA Current Source	Analog	Analog
8	IO8	DIO8	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI8	Analog Comparator 2 Positive Input (ACMP2+)	Analog	--
9	GND	GND	Ground	--	--

PIN # TQFN-14	PIN Name	Signal Name	Function	Input Options	Output Options
10	IO10	DIO10	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI10	VREF Input	Analog	--
11	IO11	DIO11	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AI11	Analog Comparator 3 Positive Input (ACMP3+)	Analog	--
12	IO12	DIO12	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		AO12	Voltage Reference Output (VREF_OUT)	--	Analog
13	IO13	DIO13	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
		EXT_OSC0_IN	External CLK of 25kHz/2MHz OSC Connection	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	--
14	IO14	DIO14	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2

Macrocell Manifest

Macrocell Name	Description	Number of Units	Total Units	Referenced Section
IOs			**12**	**5, 4.4**
Digital Input/Output	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • Open Drain Outputs: NMOS ×1(2), PMOS ×1(2) • Push Pull Outputs: PP ×1(2) • 10kΩ/100kΩ/1MΩ Pull-Up/Pull-Down resistors	• Fifteen Digital IOs	12	5
Analog Input	• Analog Input	• Seven Analog Inputs	7	5.4.1, 5.4.2, 5.5.1, 5.5.2, 5.5.4, 5.5.5, 5.5.7, 5.5.8, 5.5.9
Analog Output	• Analog Output	• One Analog Output	1	5.4.3, 5.5.10
Analog Input/Output	• Analog Input/Output	• One Analog Input/Outputs	1	5.4.2, 5.5.6
Connection Matrix			**1**	**6**
Connection Matrix	• Digital matrix connections	• Size 63×111	1	6.1, 6.2, 6.3
Multifunctional Macrocells			**27**	**7**
2-bit LUT	• 2-bit Look-Up Table	• Two 2-bit LUTs shared with DFF/LATCH w/o RST • One 2-bit LUT shared with DFF/LATCH w/o RST and 16-bit PGEN	4	7.1, 7.2
3-bit LUT	• 3-bit Look-Up Table	• Ten 3-bit LUTs shared with DFF/LATCH w/ RST • Two 3-bit LUTs shared with DFF/LATCH or 8-bit PGEN • One 3-bit LUT shared with Shift Register • Six 3-bit LUTs shared with 8-bit Timers	19	7.3, 7.4, 7.5, 7.6
4-bit LUT	• 4-bit Look-Up Table	• Two 4-bit LUTs shared with 16-bit timers • One 4-bit LUT shared with 16-bit RPGEN	3	7.7, 7.8
DFF w/o RST	• D Flip-Flop w/o RST	• Two DFFs shared with 2-bit LUTs or LATCHs w/o RST • One DFF shared with 2-bit LUT, LATCH w/o RST or 16-bit PGEN	3	7.1, 7.2
DFF w/ RST	• D Flip-Flop w/ RST	• Ten DFFs shared with 3-bit LUTs or LATCHs w/ RST • Two DFFs shared with 3-bit LUTs or LATCHs or 8-bit PGENs	12	7.3, 7.4
LATCH w/o RST	• LATCH w/o RST	• Two LATCHs shared with 2-bit LUTs or DFFs w/o RST • One LATCH shared with 2-bit LUT, DFF w/o RST or 16-bit PGEN	3	7.1, 7.2
LATCH w/ RST	• LATCH w/ RST	• Ten LATCHs shared with 3-bit LUTs or DFFs w/ RST • Two LATCHs shared with 3-bit LUTs or DFFs or 8-bit PGENs	12	7.3, 7.4
8-bit PGEN	• 8-bit Programmable Pattern Generator	• Two 8-bit PGEN shared with 3-bit LUTs or DFF/LATCH	2	7.4
16-bit PGEN	• 16-bit Programmable Pattern Generator	• One 16-bit PGEN shared with 2-bit LUT	1	7.2
16-bit RPGEN	• 16-bit Reversible Programmable Pattern Generator	• One 16-bit RPGEN shared with 4-bit LUT	1	7.8

Macrocell Name	Description	Number of Units	Total Units	Referenced Section
Shift Register	• 16 stages/3 outputs • Two outputs of 1st to 16th selectable stages • One output of 1st stage	• One Shift Register shared with 3-bit LUT	1	7.5
8-bit TMR	• 8-bit Timer	• Six 8-bit TMRs shared with 3-bit LUTs	6	7.6
16-bit TMR	• 16-bit Timer	• Two 16-bit TMRs shared with 4-bit LUTs	2	7.7
PDLY	• Programmable Delay • 140 ns/280 ns/420 ns/560 ns @ VDD = 3.30V	• One PDLY shared with Edge Detector	1	7.9
Edge Detector	• Rising Edge Detector • Falling Edge Detector • Both Edge Detector	• One Edge Detector shared with PDLY	1	7.9
Data Protection			**2**	**9**
CRC-8	• Cyclic redundancy check of NVM content	• $x^8 + x^6 + x^3 + 1$	1	9.1
CRV	• Continuous Registers Verification	• 32 bits of CRV	1	9.2
Oscillators			**2**	**10**
25kHz 2MHz	• 25 kHz or 2 MHz selectable frequency • Main prescaler: OSC/1, OSC/2, OSC/4, and OSC/8 • Two clock outputs with selectable PRESCALER_OUT: 1(OUT0), 1/2(OUT1), 1/4, 1/8, 1/16, 1/32, 1/64, 1/128(OUT0) or 1/256(OUT1)	• One OSC (25kHz/2MHz)	1	10.1, 10.2, , 4.7.1, 4.7.2
25MHz	• 25 MHz frequency • Prescaler: OSC/1, OSC/2, OSC/4, and OSC/8	• One OSC (25MHz)	1	10.1, 10.3, 4.7.3
Analog Part			**8**	**11, 12, 13, 14**
Analog Comparator	• Selectable Hysteresis 0 mV, 25 mV, Custom Hysteresis • Wake and Sleep Control (Part of Multifunctional macrocell)	• Four ACMPs	4	11, 7.7.1, 4.8
100µA Current Source	• Enabled Current Sourced connected to IO10 pad	• One 100µA Current Source	1	4.11, 14
Voltage Reference	• Used as Analog Comparators references • Can be route to IO5	• One VREF	1	12, 4.9
Analog Temperature Sensor	• Two output voltage ranges	• One TS	1	13, 4.10
POR			**1**	**15**
POR	•	•	1	15

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1. Application Examples

The AM1U1514 is a programable mixed-signal IC which can be configured and used for a wide array of applications. Below you can find four simple use cases for the AM1U1514.

Example 1.1: Power sequencer (~23% of blocks are used)

Most of the complex electronic systems have definite power supply control to ensure that every part of the system starts up properly. This example (Figure 1.2) shows the implementation of such system based on AM1U1514. IN rising event runs the two-channel start up power supply sequence and IN falling event runs power down sequence (Figure 1.1).

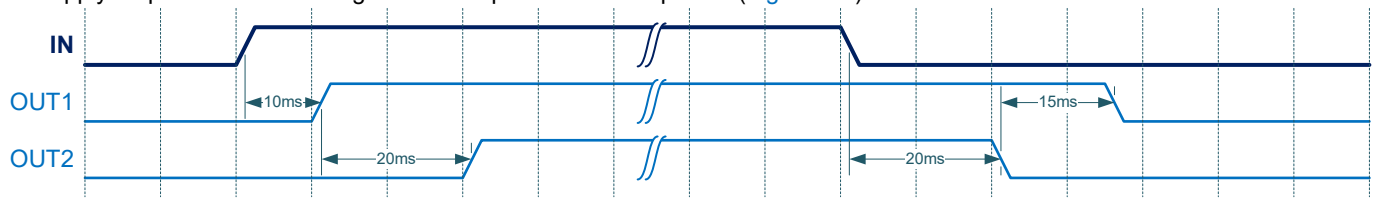


Figure 1.1. Power Sequencer requirements

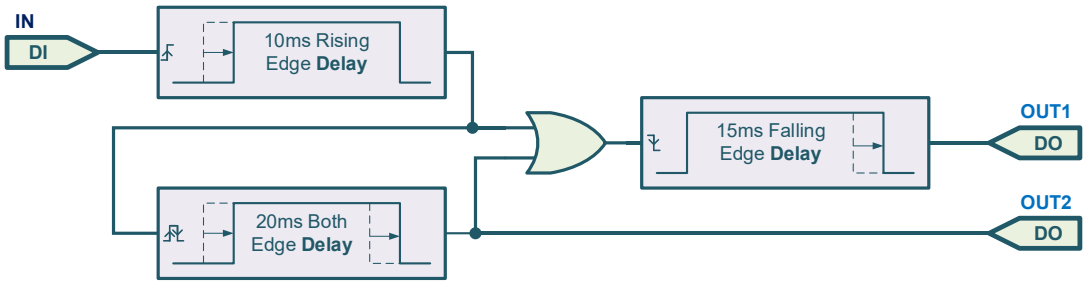


Figure 1.2. Power Sequencer implementation

Example 1.2 Watchdog timer (~18% of blocks are used)

AM1U1514 allows the customer to implement watchdog timer (Figure 1.4). If the device doesn't detect either rising or falling edge of IN signal during 100ms, it generates 500ms LOW pulse (Figure 1.3).

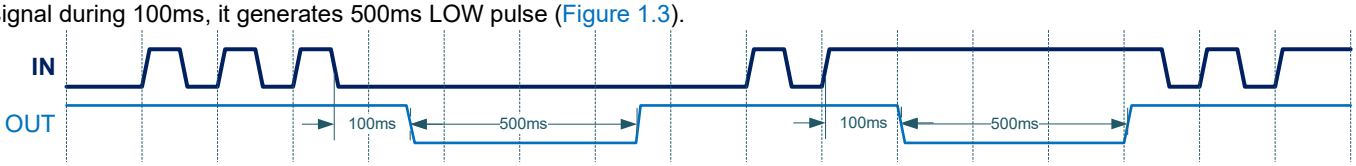


Figure 1.3. Watchdog requirements

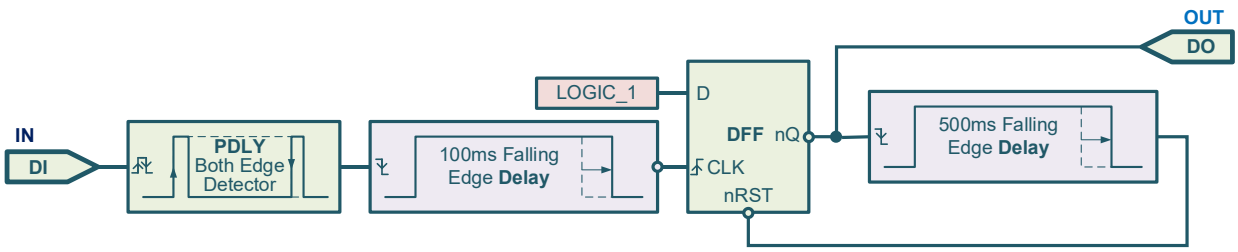


Figure 1.4. Watchdog implementation

Example 1.3 Heating Control System (~40% of blocks are used)

The current application example shows customer how to use the analog part of AM1U1514. The design can serve as the 24-hours heating control system (Figure 1.5). There are temperature sensor and analog comparators in AM1U1514, that are used to implement the system. The reference voltage of the ACMP0 set to provide so-called economical temperature of the room to minimize the heat energy consumption. ACMP1 with its reference voltage provides the comfort temperature of the room. IN+ inputs of both ACMPs are connected to the temperature sensor of the µASIC. Each timer provides the time period of economical or comfort temperature in the following sequence: TMR0 – 5hrs – economical temperature, TMR1 – 4hrs – comfort temperature, TMR2 – 8hrs – economical temperature, TMR3 – 7hrs – comfort temperature. During each time period the temperature sensor in bundle with corresponding ACMP monitors the room temperature and controls heat element (Figure 1.6), that allows to maintain the desired temperature level.

The application example uses built in Wake&Sleep controller (TMR6), to reduce power consumption of analog part (temperature sensor, voltage reference, analog comparators)

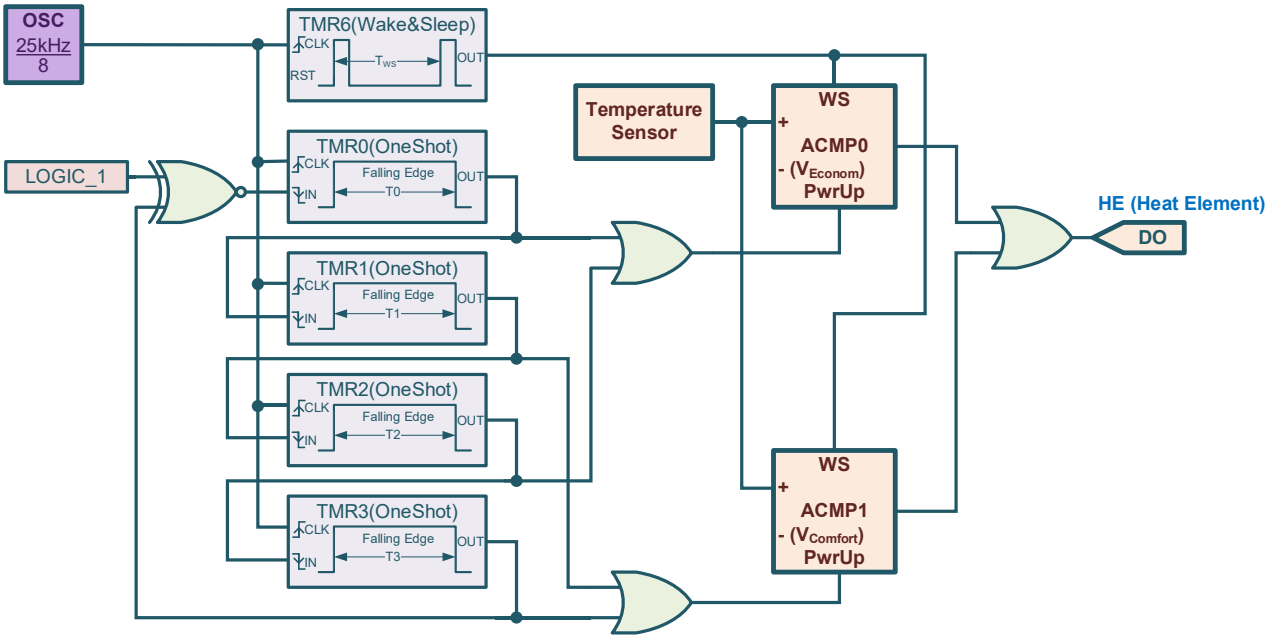


Figure 1.5. Heating Control System

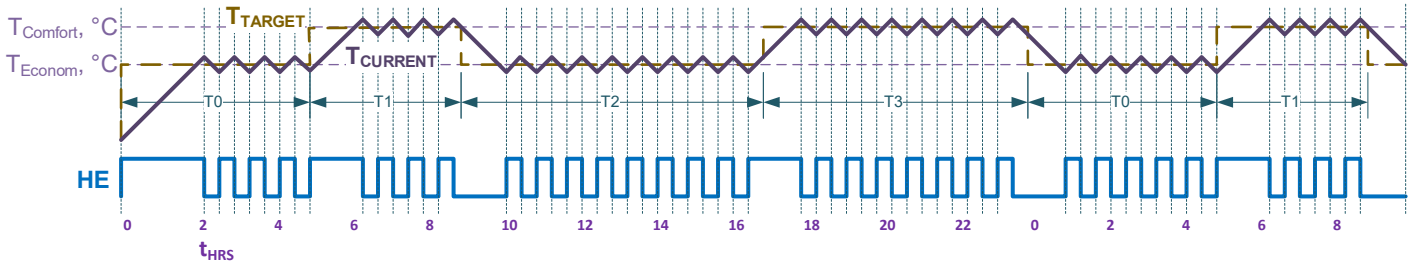


Figure 1.6. Timing Diagrams of Heating Control System

2. How to Get Samples and Go to Production

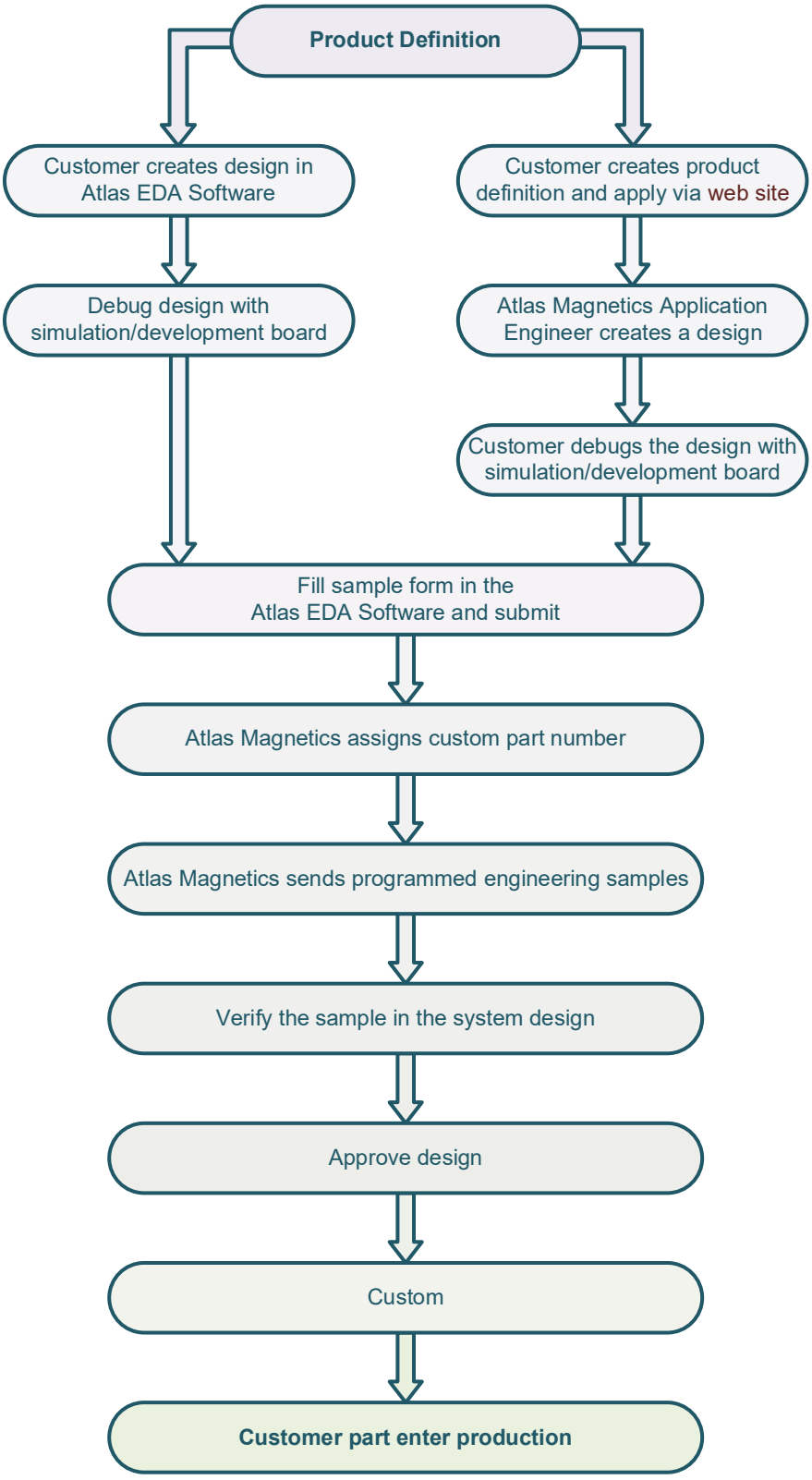


Figure 2.1. Stages of development a custom µASIC device

3. Ordering Information

3.1. Ordering Information for Unprogrammed Part

Part Number	Status	
	Unprogrammed	Programmed (Note 3.1)
AM1U1514QA	14-pin TQFN-A	14-pin TQFN-A
	14-pin TQFN-A - Tape and Reel (3k units)	14-pin TQFN-A - Tape and Reel (3k units)

Note 3.1 The custom program part number is created when design is submitted, get yours here (atlasmagnetics.com).

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Parameter		Min	Max	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage	IOs 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14	GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current Through VDD PIN			100	mA
Maximum Average or DC Current Through GND PIN			100	mA
Maximum Average or DC Current (Through pin)	PP×1	--	18	mA
	PP×2	--	28	
	OD(NMOS)×1	--	18	
	OD(NMOS)×2	--	28	
	OD(PMOS)×1	--	18	
	OD(PMOS)×2	--	28	
Current at Input PIN (Note 4.1)		-10.0	10.0	mA
Input leakage (Absolute Value)		--	5.0	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

Note 4.1 Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.71	3.30	5.50	V
T_A	Operating Temperature		-40	25	85	°C
V_O	Operating Voltage Applied to any PIN in HIGH-Impedance State		GND – 0.3	--	V_{DD}+0.3	V
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF

4.3. General Specifications

Table 4.3. General characteristics

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.66	0.90	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.47	1.56	1.64	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.35	1.46	1.54	V

4.4. IO Specifications

Table 4.4. IO Electrical Characteristics

@ V_{DD} = 1.71V to 5.50V, T = - 40 °C to +85 °C Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 4.2)	0.7xV_{DD}	--	V_{DD}+0.3	V
		Logic Input with Schmitt Trigger	0.8xV_{DD}	--	V_{DD}+0.3	V
		LOW-Level Logic Input (Note 4.2)	1.05	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 4.2)	GND-0.3	--	0.3xV_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xV_{DD}	V
		LOW-Level Logic Input (Note 4.2)	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	1.79	1.79	--	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -100 µA, V_{DD} = 1.8 V	1.79	1.80	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -100 µA, V_{DD} = 1.8 V	3.19	3.22	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -3 mA, V_{DD} = 3.3 V	3.24	3.26	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -3 mA, V_{DD} = 3.3 V	4.86	4.90	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -5 mA, V_{DD} = 5.0 V	4.93	4.95	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -5 mA, V_{DD} = 5.0 V	--	0.0022	0.0031	V
V_{OL}	LOW-Level Output Voltage	Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.0009	0.0015	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.0403	0.0479	V
		Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.0209	0.0251	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.0501	0.0606	V
		Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	0.0264	0.0322	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 5 mA, V_{DD} = 5.0 V	-2.64	-3.22	--	V
I_{OH}	HIGH-Level Output Current (see Note 4.3)	Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = V_{DD} - 0.2, V_{DD} = 1.8 V	-5.11	-6.23	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = V_{DD} - 0.2, V_{DD} = 1.8 V	-19.96	-24.58	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4, V_{DD} = 3.3 V	-36.17	-45.79	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4, V_{DD} = 3.3 V	-57.78	-66.91	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4, V_{DD} = 5.0 V	-105.39	-124.05	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4, V_{DD} = 5.0 V	3.69	4.56	--	mA
I_{OL}	LOW-Level Output Current (see Note 4.3)	Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.15 V, V_{DD} = 1.8 V	7.23	8.84	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.15 V, V_{DD} = 1.8 V	18.33	23.42	--	mA
		Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.40 V, V_{DD} = 3.3 V	35.67	44.96	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.40 V, V_{DD} = 3.3 V	25.02	32.81	--	mA
		Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.40 V, V_{DD} = 5.0 V	48.41	62.46	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.40 V, V_{DD} = 5.0 V	1.79	1.79	--	mA
R_{PULL}	Pull-Up or Pull-Down Resistance	1000 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	1000	--	kΩ

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
		100 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	100	--	kΩ
		10 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance		--	4	10	pF
Note 4.2	*No hysteresis*					
Note 4.3	*DC or average current through any pin should not exceed value given in Absolute Maximum Conditions*					

4.5. Typical Current Consumption

Table 4.5. Typical Current Consumption for Each Macrocell

Symbol	Parameter	Note	VDD = 1.8 V	VDD = 3.3 V	VDD = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent	0.40	0.42	0.47	µA
		OSC 2 MHz, OFF State	--	--	<1	nA
		OSC 2 MHz, IDLE State	212.93	213.99	215.78	nA
		OSC 2 MHz, PreScaler = 1	5.35	10.60	17.46	µA
		OSC 2 MHz, PreScaler = 2	4.38	8.78	14.58	µA
		OSC 2 MHz, PreScaler = 4	3.85	7.80	13.03	µA
		OSC 2 MHz, PreScaler = 8	3.61	7.35	12.31	µA
		OSC 25 kHz, OFF State	--	--	<1	nA
		OSC 25 kHz, IDLE State	214.27	200	210	nA
		OSC 25 kHz, PreScaler = 1	0.18	0.28	0.40	µA
		OSC 25 kHz, PreScaler = 2	0.17	0.25	0.36	µA
		OSC 25 kHz, PreScaler = 4	0.16	0.24	0.34	µA
		OSC 25 kHz, PreScaler = 8	0.16	0.24	0.33	µA
		OSC 25 MHz, OFF State	--	--	<1	nA
		OSC 25 MHz, IDLE State	280.82	282.60	287.32	nA
		OSC 25 MHz, PreScaler = 1	60.30	102.13	151.33	µA
		OSC 25 MHz, PreScaler = 2	49.19	81.61	119.31	µA
		OSC 25 MHz, PreScaler = 4	43.36	70.71	102.24	µA
		OSC 25 MHz, PreScaler = 8	40.66	65.68	94.31	µA
		VREF(50 mV – 1200 mV): internal	4.04	4.00	4.32	µA
		VREF(VDD)	3.6	6.3	8.7	µA
		VREF(50mV – 1200mV): external IO	18.5	18.5	18.8	µA
		VREF(VDD): external IO	18.1	20.8	23.3	µA
		ACMP (high speed mode w/ buffer)	12.11	12.33	13.20	µA
		ACMP (high speed mode w/o buffer)	9.45	9.65	10.39	µA
		ACMP (low power mode w/ buffer)	3.78	3.81	4.01	
		ACMP (low power mode w/o buffer)	1.12	1.14	1.20	
		VREF(50 mV – 1200 mV): internal	7.1	7.2	7.2	
		100µA Current Source	4.41	4.05	4.17	µA
		Temperature sensor ON	0.40	0.42	0.47	µA

4.6. Timing Estimator

Table 4.6 Typical Propagation Time for IOs

Start Point	End point	Note	VDD = 1.71 V		VDD = 3.3 V		VDD = 5.5 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
DI w/o ST	DO PP×1	IO	58.76	43.27	17.13	14.40	10.43	9.89	ns
DI w/o ST	DO PP×2	IO	58.36	44.22	16.95	14.25	10.32	9.80	ns
DI w/ ST	DO PP×1	IO	62.41	48.11	19.67	16.28	12.63	11.15	ns
DI w/ ST	DO PP×2	IO	61.96	47.74	19.49	16.13	12.55	11.03	ns
DI LV	DO PP×1	IO	39.83	73.39	11.48	28.91	6.08	26.12	ns
DI LV	DO PP×2	IO	39.46	73.02	11.33	28.04	6.12	26.08	ns

Table 4.7 Typical Propagation Time for Each Macrocell

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		VDD = 5.0 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
IN	OUT	2-bit LUT	24.30	26.18	8.25	8.97	5.63	6.03	ns
IN	OUT	3-bit LUT	28.19	30.11	9.54	10.30	6.49	6.91	ns
IN	OUT	4-bit LUT	25.93	28.23	8.80	9.67	5.97	6.47	ns
CLK	Q	DFF w/o nRST(nSET)	30.69	30.86	10.50	11.58	6.44	7.59	ns
CLK	nQ	DFF w/o nRST(nSET)	31.51	30.38	13.13	10.54	6.62	7.44	ns
CLK	Q	DFF w/ nRST(nSET)	29.55	30.46	9.92	10.18	6.15	7.35	ns
nRST	Q	DFF w/ nRST	--	33.85	--	12.05	--	7.36	ns
nSET	Q	DFF w/ nSET	33.65	--	11.04	--	7.86	--	ns
RST	Q	DFF w/ nRST	--	33.40	--	10.95	--	7.86	ns
SET	Q	DFF w/ nSET	33.24	--	11.48	--	7.04	--	ns
CLK	nQ	DFF w/ nRST(nSET)	30.84	29.92	10.46	10.46	6.41	7.16	ns
nRST	nQ	DFF w/ nRST	33.86	--	11.08	--	7.88	--	ns
nSET	nQ	DFF w/ nSET	--	33.97	--	12.10	--	7.46	ns
RST	nQ	DFF w/ nRST	33.27	--	11.46	--	7.00	--	ns
SET	nQ	DFF w/ nSET	--	33.55	--	11.04	--	7.95	ns
D	Q	LATCH w/o nSET	31.33	29.89	10.78	11.35	6.39	7.15	ns
nL	Q	LATCH w/o nSET	31.83	25.48	10.97	9.80	6.47	7.60	ns
D	nQ	LATCH w/o nSET	37.43	24.62	11.71	9.49	8.20	7.31	ns
nL	nQ	LATCH w/o nSET	32.79	25.24	11.29	9.83	6.67	7.43	ns
D	Q	LATCH w/ nSET	23.89	26.52	7.79	8.66	5.13	5.44	ns
nL	Q	LATCH w/ nSET	27.11	23.38	9.24	9.08	5.90	6.80	ns
nSET	Q	LATCH w/ nSET	29.91	--	10.14	--	7.34	--	ns
SET	Q	LATCH w/ nSET	29.54	--	10.21	--	6.24	--	ns
D	nQ	LATCH w/ nSET	31.12	19.49	9.78	7.84	6.61	5.83	ns
nL	nQ	LATCH w/ nSET	28.26	22.77	9.79	8.89	6.09	6.67	ns
nSET	nQ	LATCH w/ nSET	--	30.06	--	10.35	--	6.32	ns
SET	nQ	LATCH w/ nSET	--	29.78	--	10.13	--	7.29	ns
CLK	OUT0	Shift register	36.02	27.53	9.06	6.85	4.00	4.21	ns
CLK	OUT1	Shift register	34.19	26.58	8.40	6.49	3.48	4.14	ns
CLK	Q[1]	Shift register	28.21	20.54	6.84	5.12	2.00	2.91	ns
CLK	nOUT1	Shift register	32.18	27.14	8.28	6.80	3.20	4.25	ns
nRST	OUT0	Shift register	--	30.73	--	8.35	--	3.74	ns
nRST	OUT1	Shift register	--	29.76	--	8.11	--	3.39	ns
nRST	Q[1]	Shift register	--	23.90	--	6.25	--	2.22	ns
nRST	nOUT1	Shift register	35.84	--	8.39	--	4.22	--	ns
IN	OUT	8-bit TMR (Delay)	40.27	40.42	13.63	14.23	8.88	9.43	ns
IN	OUT	8-bit TMR (One-Shot)	50.63	51.83	17.20	17.69	11.24	11.33	ns
IN(RST)	OUT	8-bit TMR (Counter)	53.82	55.12	18.28	18.77	11.90	12.01	ns
IN	OUT	8-bit TMR (Frequency Detector)	48.30	49.56	16.52	17.02	10.80	10.94	ns
IN	OUT	8-bit TMR (Edge Detector)	39.68	40.89	13.39	13.87	8.65	8.88	ns
CLK	OUT	8-bit TMR (Delay)	63.14	61.97	21.36	21.30	13.75	13.92	ns
CLK	OUT	8-bit TMR (One-Shot)		60.55		20.86		13.66	ns
CLK	OUT	8-bit TMR (Counter)	59.81	58.14	20.16	20.43	12.97	13.59	ns
CLK	OUT	8-bit TMR (Frequency Detector)	--	59.39	--	20.41	--	13.30	ns
IN	OUT	16-bit TMR (Delay)	52.28	53.98	17.90	18.52	11.81	11.95	ns
IN	(OUT	16-bit TMR (One-Shot)	45.56	47.44	15.43	16.10	10.07	10.31	ns
IN(RST)	OUT	16-bit TMR (Counter)	52.28	53.98	17.90	18.52	11.81	11.95	ns
IN	OUT	16-bit TMR (Frequency Detector)	43.22	44.88	14.69	15.39	9.60	9.88	ns
IN	OUT	16-bit TMR (Edge Detector)	34.73	36.40	11.69	12.27	7.54	7.88	ns
CLK	OUT	16-bit TMR (Delay)	72.86	72.21	24.61	24.81	15.88	16.36	ns
CLK	OUT	16-bit TMR (One-Shot)	--	70.92	--	24.42	--	16.15	ns
CLK	OUT	16-bit TMR (Counter)	69.47	69.18	23.46	23.97	15.13	15.86	ns

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		VDD = 5.0 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
CLK	OUT	16-bit TMR (Frequency Detector)	--	69.50	--	23.87	--	15.70	ns
CLK	OUT	16-bit PGEN	23.00	36.00	8.00	11.00	5.00	7.00	ns
RST	OUT	16-bit PGEN	16.00	28.00	7.00	10.00	5.00	6.00	ns
CLK	OUT	8-bit PGEN	22.50	35.50	8.00	11.00	5.00	6.50	ns
RST	OUT	8-bit PGEN	27.50	38.50	9.50	11.50	6.00	7.00	ns
nRST	OUT	8-bit PGEN	16.50	27.50	7.00	9.50	5.00	6.00	ns
CLK	OUT	16-bit RPGEN	22.00	35.00	8.00	11.00	5.00	7.00	ns
RST	OUT	16-bit RPGEN	17.00	28.00	7.00	10.00	5.00	6.00	ns
nRST	OUT	16-bit RPGEN	24.00	38.00	9.00	12.00	6.00	7.00	ns

Table 4.8 Expected Delays and Widths for Programmable Delay/Edge Detector

Symbol	Parameter	Note	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
T_{Width}	Width, 1 cell	Mode:(any)Edge Detect, Edge Detect Output	203.58	166.31	160.75	ns
T_{Width}	Width, 2 cells	Mode:(any)Edge Detect, Edge Detect Output	299.19	313.72	344.53	ns
T_{Width}	Width, 3 cells	Mode:(any)Edge Detect, Edge Detect Output	397.30	461.70	528.52	ns
T_{Width}	Width, 4 cells	Mode:(any)Edge Detect, Edge Detect Output	495.28	609.64	713.28	ns
T_{PROP}	Delay, 1 cell	Mode:(any)Edge Detect, Edge Detect Output	24.51	8.35	5.59	ns
T_{PROP}	Delay, 2 cells	Mode:(any)Edge Detect, Edge Detect Output	24.55	8.41	5.65	ns
T_{PROP}	Delay, 3 cells	Mode:(any)Edge Detect, Edge Detect Output	24.66	8.44	5.64	ns
T_{PROP}	Delay, 4 cells	Mode:(any)Edge Detect, Edge Detect Output	24.68	8.47	5.68	ns
T_{DLY}	Delay, 1 cell	Mode: Both Edge Delay, Edge Detect Output	244.44	181.48	168.95	ns
T_{DLY}	Delay, 2 cells	Mode: Both Edge Delay, Edge Detect Output	419.38	359.64	366.60	ns
T_{DLY}	Delay, 3 cells	Mode: Both Edge Delay, Edge Detect Output	580.11	533.33	563.88	ns
T_{DLY}	Delay, 4 cells	Mode: Both Edge Delay, Edge Detect Output	737.45	705.07	760.15	ns

4.7. OSC Specifications

4.7.1. 25 kHz Oscillator

Table 4.9 25 kHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Min, kHz	Max, kHz	Min, kHz	Max, kHz
1.8 V ±5%	24.70	25.28	22.51	27.99
3.3 V ±10%	24.70	25.29	22.50	27.97
5 V ±10%	24.71	25.28	22.57	28.41
2.5 V…4.5 V	24.71	25.34	22.53	27.95
2.3 V…5.5 V	24.71	25.75	22.53	28.38
1.71 V…5.50 V	24.68	25.31	22.51	28.41

Table 4.10 25 kHz OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max
1.8 V ±5%	-1.20%	1.12%	-9.95%	11.96%
3.3 V ±10%	-1.20%	1.16%	-10.00%	11.88%
5 V ±10%	-0.92%	3.00%	-9.72%	13.64%
2.5 V…4.5 V	-1.16%	1.36%	-9.88%	11.80%
2.3 V…5.5 V	-1.16%	3.00%	-9.88%	13.52%
1.71 V…5.50 V	-1.20%	3.05%	-9.95%	13.64%

Table 4.11 25 kHz OSC Power on time at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.71	355.04	486.11	24.13	77.78
1.80	353.33	454.02	18.81	80.52
3.30	341.67	451.24	21.35	85.08
5.00	325.01	428.47	20.11	78.38
5.50	308.40	412.89	21.32	74.49

Table 4.12 25 kHz OSC Frequency Settling Time

Parameter	Description	Typ	Max	Unit
Frequency Settling Time (Normal mode)	To reach the 2.5% error	1	1	Cycles
Frequency Settling Time (Fast mode)	To reach the 2.5% error	1	1	Cycles

4.7.2. 2 MHz Oscillator

Table 4.13 2 MHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Min, MHz	Max, MHz	Min, MHz	Max, MHz
1.8 V ±5%	1.97	2.03	1.85	2.16
3.3 V ±10%	1.97	2.03	1.86	2.16
5 V ±10%	1.97	2.03	1.85	2.17
2.5 V…4.5 V	1.96	2.04	1.85	2.16
2.3 V…5.5 V	1.96	2.06	1.85	2.17
1.71 V…5.50 V	1.96	2.06	1.85	2.18

Table 4.14 2 MHz OSC Frequency Error (Error Calculated in Relation to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max
1.8 V ±5%	-1.42%	1.28%	-7.19%	7.52%
3.3 V ±10%	-1.42%	1.31%	-6.89%	7.80%
5 V ±10%	-1.79%	2.73%	-7.13%	8.47%
2.5 V - 4.5 V	-2.00%	2.00%	-7.50%	8.00%
2.3 V…5.5 V	-2.00%	3.00%	-7.50%	8.50%
1.71 V…5.50 V	-1.80%	2.90%	-7.20%	8.68%

Table 4.15 2 MHz OSC Power on time at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.71	72.88	91.06	0.51	1.13
1.80	72.52	91.08	0.49	1.24
3.30	64.56	81.03	0.37	1.12
5.00	55.49	69.40	0.34	1.10
5.50	51.57	64.30	0.32	0.93

Table 4.16 2 MHz OSC Frequency Settling Time

Parameter	Description	Typ	Max	Unit
Frequency Settling Time (Normal mode)	To reach the 2.5% error	2	5	Cycles
Frequency Settling Time (Fast mode)	To reach the 2.5% error	3	6	Cycles

4.7.3. 25 MHz Oscillator

Table 4.17 25 MHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Min, MHz	Max, MHz	Min, MHz	Max, MHz
1.8 V ±5%	24.66	25.31	22.93	27.63
3.3 V ±10%	24.61	25.35	22.90	27.64
5 V ±10%	24.11	25.64	22.67	27.79
2.5 V - 4.5 V	24.28	25.71	22.77	27.81
2.3 V…5.5 V	24.10	25.82	22.64	27.83
1.71 V…5.50 V	24.09	26.13	22.63	28.13

Table 4.18 25 MHz OSC Frequency Error (Error Calculated in Relation to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max
1.8 V ±5%	-1.35%	1.24%	-8.26%	10.49%
3.3 V ±10%	-1.54%	1.39%	-8.39%	10.54%
5 V ±10%	-3.54%	2.56%	-9.31%	11.13%
2.5 V…4.5 V	-2.88%	2.84%	-8.92%	11.24%
2.3 V…5.5 V	-3.60%	3.28%	-9.44%	11.32%
1.71 V…5.50 V	-3.62%	4.52%	-9.45%	12.51%

Table 4.19 25 MHz OSC Power On Delay at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.71	40.22	50.36	0.18	0.25
1.80	40.12	50.37	0.16	0.24
3.30	38.88	48.74	0.07	0.14
5.00	37.51	46.87	0.06	0.14
5.50	36.75	45.73	0.06	0.15

Table 4.20 25 MHz OSC Frequency Settling Time

Parameter	Description	Typ	Max	Unit
Frequency Settling Time (Normal mode)	To reach the 2.5% error	12	25	Cycles
Frequency Settling Time (Fast mode)	To reach the 2.5% error	12	26	Cycles

4.8. ACMP Specifications

Table 4.21 ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD} – 0.3	V
V_{OFFSET}	ACMP Input Offset Voltage	Low Power Mode, V_{HYS} = 0 mV, Gain = 1, V_{REF} = (50…1200) mV, V_{DD} = (1.71…5.50) V	T = 25°C	-7.58	--	10.07	mV
			T = (-40…85)°C	-8.08	--	10.29	mV
		High Speed Mode, V_{HYS} = 0 mV, Gain = 1, V_{REF} = (50...1200) mV, V_{DD} = (1.71…5.50) V	T = 25°C	-5.01	--	6.68	mV
			T = (-40...85)°C	-5.72	--	7.06	mV
V_{HYS}	ACMP 25mV hysteresis	Low Power Mode, Gain = 1, V_{REF} = (50...1200, VDD-0.4) mV, V_{DD} = (1.71…5.50) V	T = 25°C	7.45	25	31.06	mV
			T = (-40...85)°C	4.48	25	47.01	mV
		High Speed Mode, Gain = 1, V_{REF} = (50...1200, VDD-0.4) mV, V_{DD} = (1.71…5.50) V	T = 25°C	8.50	25	27.56	mV
			T = (-40...85)°C	6.70	25	33.79	mV
t_{START}	ACMP Power On Time	ACMP Power on time, Minimal required wake time for the "Wake and Sleep function"	T = 25°C	--	96.70	172.60	µs
			T = (-40…85)°C	--	96.87	192.30	µs
R_{SIN}	Series Input Resistance	GAIN = 1×		1000.00	--	--	MΩ
		GAIN ≠ 1		1.92	2.04	2.16	MΩ
t_{PROP}	Propagation Delay, Response Time	Low Power Mode, Gain = 1, Overdrive = 10 mV V_{REF} = (50…1200) mV	Low to High T = 25°C	--	17.80	39.46	µs
			High to Low T = 25°C	--	17.62	42.49	µs
			Low to High T = (-40...+85)°C	--	11.21	42.07	µs
			High to Low T = (-40...+85)°C	--	11.16	42.49	µs
		High Spee Mode, Gain = 1, Overdrive = 10 mV V_{REF} = (50…1200) mV	Low to High T = 25°C	--	0.95	2.02	µs
			High to Low T = 25°C	--	0.96	2.04	µs
			Low to High T = (-40...+85)°C	--	0.59	2.02	µs
			High to Low T = (-40...+85)°C	--	0.60	2.04	µs
		Low Power Mode, Gain = 1, Overdrive = 100 mV V_{REF} = (50…1200) mV	Low to High T = 25°C	--	4.10	15.81	
			High to Low T = 25°C	--	4.96	20.14	
			Low to High T = (-40...+85)°C	--	4.18	17.87	
			High to Low T = (-40...+85)°C	--	5.04	20.14	
		High Spee Mode, Gain = 1, Overdrive = 100 mV V_{REF} = (50…1200) mV	Low to High T = 25°C	--	0.20	0.52	
			High to Low T = 25°C	--	0.20	0.55	
			Low to High T = (-40...+85)°C	--	0.21	1.19	

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
			High to Low T = (-40...+85)°C	--	0.21	1.34	
G	Gain	G = 1		--	1.00	--	
		G = 0.5		0.49	0.50	0.52	
		G = 0.33		0.32	0.33	0.35	
		G = 0.25		0.24	0.25	0.27	

4.9. Voltage Reference Specification

Table 4.22 VREF Specifications

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
ΔV_{REF}	Internal V_{REF} error	V_{DD} = 1.71 V	T = 25°C	-0.91	--	1.06	%
			T = (-40...85)°C	-1.68	--	1.18	%
		V_{DD} = 3.3 V	T = 25°C	-0.76	--	1.09	%
			T = (-40…85)°C	-1.67	--	1.15	%
		V_{DD} = 5.5 V	T = 25°C	-0.85	--	1.03	%
			T = (-40…85)°C	-1.72	--	1.42	%
$\Delta V_{REF\ OUT}$	Output V_{REF} error (Buffered)	V_{DD} = 1.71 V Loading is 1µA	T = 25°C	-1.32	--	1.73	%
			T = (-40...85)°C	-2.14	--	1.75	%
		V_{DD} = 3.3 V Loading is 1µA	T = 25°C	-1.25	--	1.59	%
			T = (-40…85)°C	-1.92	--	1.70	%
		V_{DD} = 5.5 V Loading is 1µA	T = 25°C	-2.74	--	1.03	%
			T = (-40…85)°C	-3.64	--	1.42	%
$C_{VREF\ OUT}$	Output Capacitance Loading	R_{LR} – Load Resistance	R_{LR} = 1MΩ	--	--	25	pF
R_{VDD_DIV}	VDD Divider Stage Input Resistance	VDD Divider is 1/2		--	500.0	--	kΩ
		VDD Divider is 1/3		--	500.0	--	kΩ
		VDD Divider is 1/4		--	500.0	--	kΩ
R_{EXT_DIV}	External VREF (IO10) Divider Stage Input Resistance	External Divider is 1		--	100.0	--	MΩ
		External Divider is 1/2		--	500.0	--	kΩ
		External Divider is 1/3		--	500.0	--	kΩ
		External Divider is 1/4		--	500.0	--	kΩ

4.10. Analog Temperature Sensor (TS) Specifications

Table 4.23 Analog Temperature Sensor Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TS_{OUT}	Temperature Sensor Output	Range 1	622.73	810.18	1016.35	mV
		Range 2	758.87	987.59	1240.16	mV
TS_{OUT_ERROR}	Temperature Sensor Output Error	Range 1	-11.74	--	+11.75	mV
		Range 2	-16.31	--	+12.79	mV
$TS_{OUT\_ACCURACY}$	Temperature Sensor Accuracy	Range 1	-4.28	--	+4.29	°C
		Range 2	-3.79	--	+4.84	°C
TS_{OUT_Slope}	Temperature Sensor Output Slope	Range 1	-2.89	-2.74	-2.60	mV/°C
		Range 2	-3.56	-3.37	-3.19	mV/°C
T_{PWR_ON}	Temperature Sensor Power On Time		--	19.86	35.24	µs

4.11. 100µA Current Source Specifications

Table 4.24 Current Source Electrical Characteristics

Symbol	Parameter	Condition/Note	Min	Typ	Max	Unit
I_O	Output Current	V_{DD} = 1.71, V_{IO} = 0…V_{DD}-0.3V T = 25°C	87.44	98.38	110.14	µA
		V_{DD} = 1.71, V_{IO} = 0…V_{DD}-1.0V T = 25°C	91.26	100.70	110.14	µA
		V_{DD} = 3.3, V_{IO} = V_{DD}-0.7V T = 25°C	86.72	95.41	104.11	µA
		V_{DD} = 5.5, V_{IO} = V_{DD}-0.7V T = 25°C	84.21	92.74	101.27	µA
		V_{DD} = 1.71, V_{IO} = V_{DD}-0.7V T = (-40…85)°C	82.82	98.43	113.99	µA
		V_{DD} = 3.3, V_{IO} = V_{DD}-0.7V T = (-40…85)°C	80.64	95.68	111.05	µA
		V_{DD} = 5.5, V_{IO} = V_{DD}-0.7V T = (-40…85)°C	78.56	92.99	108.15	µA
R_{OUT}	Output Impedance	T = 25°C	--	0.67	--	MΩ
		T = (-40…85)°C	--	0.67	--	MΩ

5. IO PINs

5.1. Input Modes

Each of the IOs can be configured as a Digital Input with or without a buffered Schmitt trigger or they can also be configured as a Digital Input Low Voltage. IO13 can be configured as External CLK Connection. IO2, IO3, IO5, IO6, IO7, IO8, IO10, and IO11 can be configured as Analog Inputs.

5.2. Output Modes

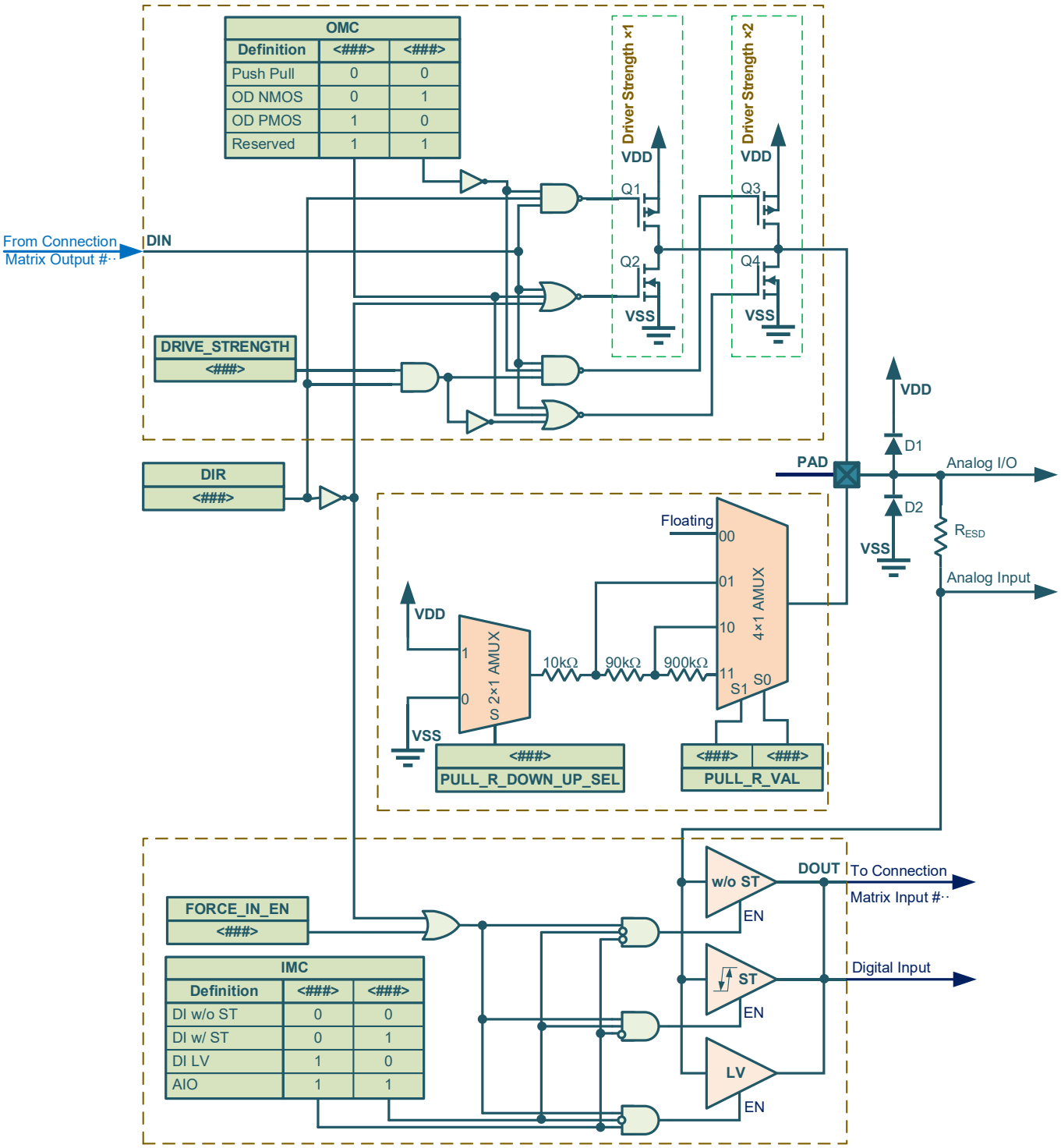
All IOs except can be configured as digital outputs. IO12 can output V_{REF}.

5.3. Pull Up/Down Resistors

All IOs have an option for user selectable resistors connected to the input structure, with the selectable values being 10 kΩ, 100 kΩ and 1 MΩ. The internal resistors can be configured as pull-up or pull-down.

5.4. IO Structures

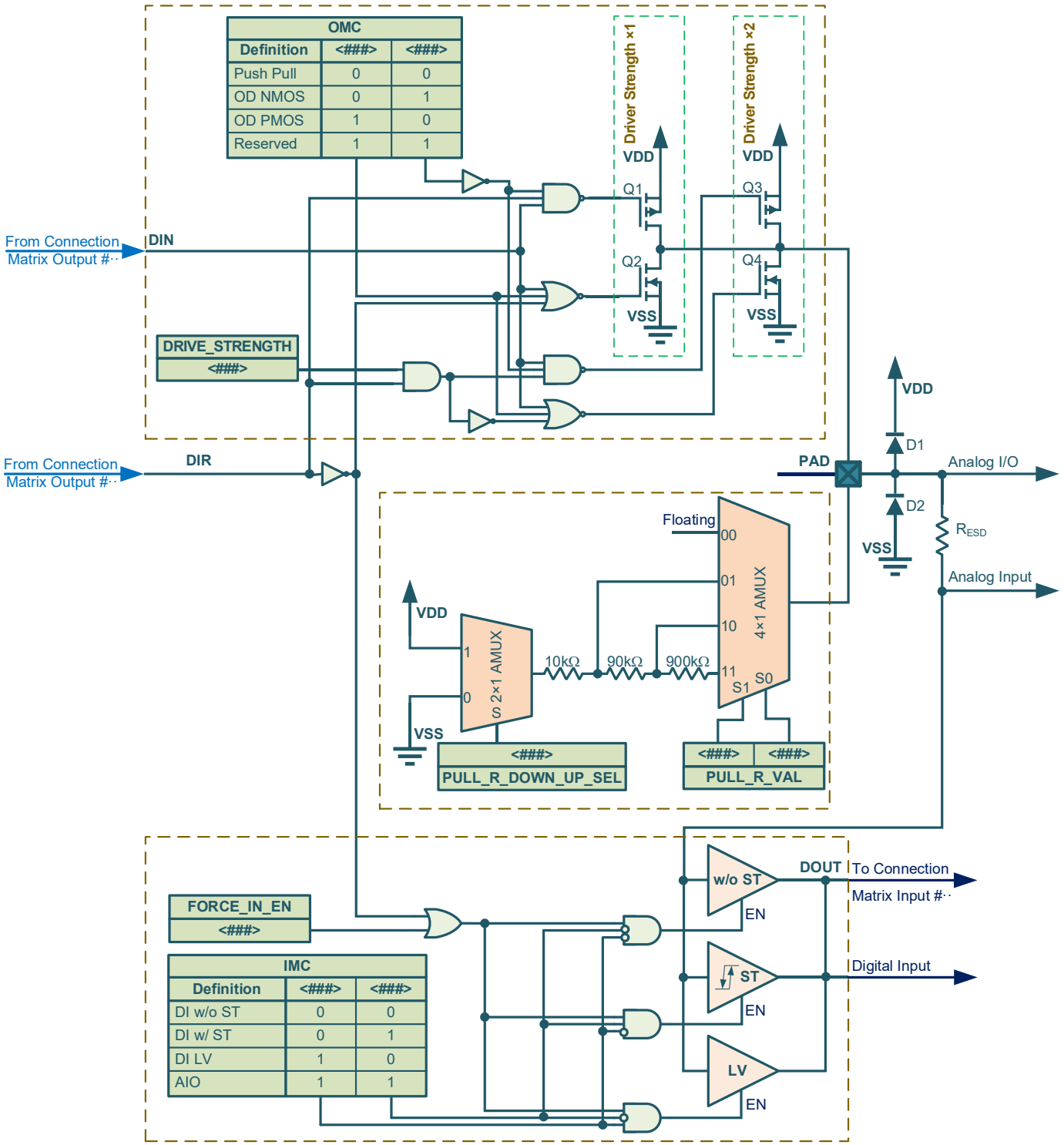
5.4.1. IO (with DIR controlled by Register) Structure (IO2, IO3, IO5, IO8, IO11)



IO#	Analog IO	Analog Input	Digital Input	DIN	DOUT
IO2	--	ACMP1 IN+	--	CMO87	CMI49
IO3	--	ACMP2 IN+	--	CMO85	CMI52
IO5	--	ACMP0 IN+	--	CMO90	CMI51
IO8	--	ACMP2 IN+	--	CMO98	CMI55
IO11	--	ACMP3 IN+	--	CMO102	CMI57

Figure 5.1. IO (with DIR controlled by Register) Structure Diagram (IO2, IO3, IO5, IO8, IO11)

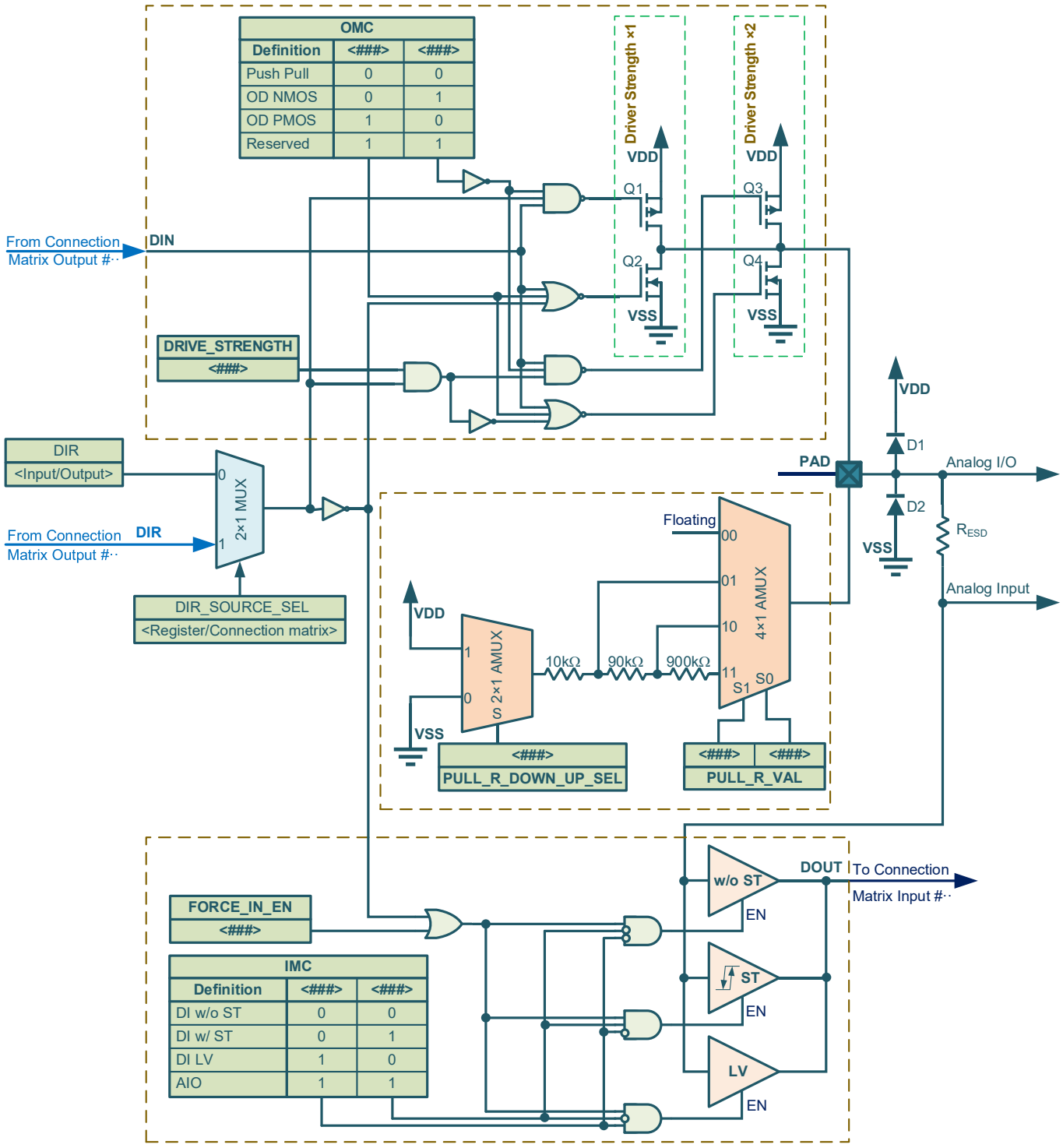
5.4.2. IO (with DIR controlled by Connection Matrix) Structure (IO4, IO6, IO7, IO10, IO13, IO14)



IO#	Analog IO	Analog Input	Digital Input	DIN	DIR	DOUT
IO4	--	--	--	CMO103	CMO104	CMI58
IO6	--	ACMP# IN-	--	CMO91	CMO92	CMI52
IO7	100µA Current Source OUT	ACMP1 IN+	--	CMO95	CMO96	CMI53
IO10	--	VREF Input	--	CMO100	CMO101	CMI56
IO13	--	--	OSC0 EXT_CLK	CMO106	CMO107	CMI60
IO14	--	--	--	CMO108	CMO109	CMI61

Figure 5.2. IO (with DIR controlled by Connection Matrix) Structure Diagram (IO7, IO10, IO13, IO14, IO16, IO18, IO19)

5.4.3. IO (with DIR controlled by Connection Matrix or Register) Structure (IO12)



IO#	Analog IO	Analog Input	DIN	DIR	DOUT
IO12	VREF OUT	--	CMO88	CMO89 (shared with VREF PWR_ON and TS PWR_ON)	CMI53

Figure 5.3. IO (with DIR controlled by Connection Matrix or Register) Structure Diagram (IO3, IO5)

5.5. IO Registers

5.5.1. IO2 Registers

Table 5.1 IO2 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO2				
0x3200	<0>	IO2_CONF	DIR	Direction: 0: Input 1: Output
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x3201	<0>	IO2_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.2. IO3 Registers

Table 5.2 IO3 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO3				
0x3100	<0>	IO3_CONF0		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x2056	<0>	IO3_CONF1	DIR	Direction: 0: Input 1: Output
	<7:1>			Reserved
0x3101	<0>	IO3_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<4:3>			Reserved
	<5>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7:6>			Reserved

5.5.3. IO4 Registers

Table 5.3 IO4 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO4				
0x3D00	<0>	IO4_CONF		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x3D01	<0>	IO4_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<5:3>			Reserved
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7>			Reserved

5.5.4. IO5 Registers

Table 5.4 IO5 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO5				
0x3400	<0>	IO5_CONF	DIR	Direction: 0: Input 1: Output
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Driver strength: 0: ×1 1: ×2
	<7>			Reserved
0x3401	<0>	IO5_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.5. IO6 Registers

Table 5.5 IO6 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO6				
0x3500	<0>	IO6_CONF		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
0x3501	<0>	IO6_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<4:3>			Reserved
	<5>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7:6>			Reserved

5.5.6. IO7 Registers

Table 5.6 IO7 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO7				
0x3800	<0>	IO7_CONF		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog IO
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x3801	<0>	IO7_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<3>			Reserved
	<4>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7:5>			Reserved

5.5.7. IO8 Registers

Table 5.7 IO8 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO8				
0x3A00	<0>	IO8_CONF0		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x2063	<0>	IO8_CONF1	DIR	Direction: 0: Input 1: Output
	<7:1>			Reserved
0x3A01	<0>	IO8_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.8. IO10 Registers

Table 5.8 IO10 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO10				
0x3B00	<0>	IO10_CONF		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x3B01	<0>	IO10_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.9. IO11 Registers

Table 5.9 IO11 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO11				
0x3C00	<0>	IO11_CONF	DIR	Direction: 0: Input 1: Output
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Input
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x3C01	<0>	IO11_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.10. IO12 Registers

Table 5.10 IO12 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO12				
0x3300	<0>	IO12_CONF	DIR	Direction: 0: Input 1: Output
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Analog Output
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Driver strength: 0: ×1 1: ×2
	<7>		DIR_SOURCE_SEL	Direction source selection: 0: Register 1: Connection matrix
0x3301	<0>	IO12_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.11. IO13 Registers

Table 5.11 IO13 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO13				
0x3F00	<0>	IO13_CONF		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<6>		DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
	<7>			Reserved
0x3F01	<0>	IO13_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

5.5.12. IO14 Registers

Table 5.12 IO14 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
IO14				
0x4000	<0>	IO14_CONF		Reserved
	<1>		FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
	<3:2>		IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
	<5:4>		OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
	<6>		DRIVE_STRENGTH	Driver strength: 0: ×1 1: ×2
	<7>			Reserved
0x4001	<0>	IO14_PULL_R	DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
	<2:1>		VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
	<7:3>			Reserved

6. Connection Matrix

The AM1U1514 Connection Matrix is used to create internal routing between cells what in turn allows to get customized functionality of the device. All of the connections of each cell within the AM1U1216 are defined by the value of corresponding register bits, which values is loaded from NVM during power up of the device.

The Connection Matrix has 63 inputs and 111 outputs. Each individual input to the Connection Matrix is hard-wired to a particular macrocell output: including IOs, Multifunctional Macrocells, Logic **1**, Logic **0,** etc. Each individual output from the Connection Matrix is hard-wired to a particular macrocell input and uses a 6-bit register to select one of the 63 input lines (see Section 6.1. Example of Connection).

6.1. Example of Connection Matrix

A simple design example to showcase the Matrix Connection is shown in the Figure 6.1.

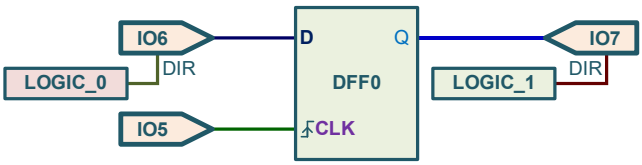


Figure 6.1. Example Design

Figure 6.2 and Figure 6.3 explain the strategy of Connection Matrix configuration.

Function	IN	Logic 0	Logic 1	DFF0 (Q)	MF1 (OUT)	. . .	. . .	. . .	IO5 (DOUT)	IO6 (DOUT)	IO7 (DOUT)	. . .	Re-served
OUT	#	00	01	02	03	. . .	. . .	. . .	51	52	53	. . .	62
DFF0(CLK) 0×2000	00												
DFF0(D) 0×2001	01												
MF1(IN0) 0×2002	02												
MF1(IN1) 0×2003	03												
. .	. .												
IO6(DIN) 0x205C	92												
. .	. .												
IO7(DIN) 0×205F	95												
IO7(DIR) 0×2060	96												
. .	. .												
IO14(DIN) 0×206B	108												
IO14(DIR) 0×206D	109												
Reserved 0×206E	110												

Figure 6.2. Connection Matrix Structure

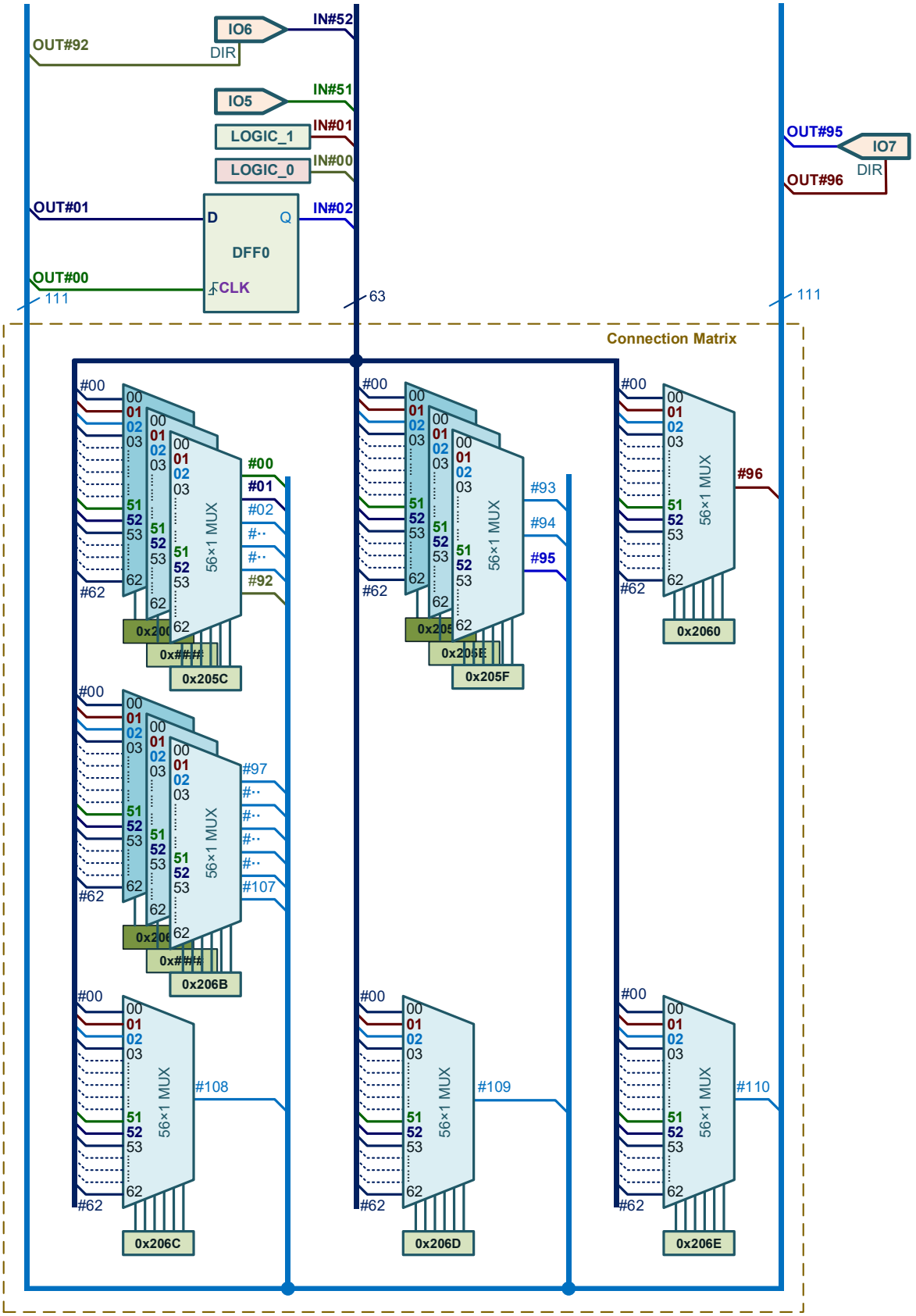


Figure 6.3. Block Diagram of Connection Matrix

6.2. Matrix Input

Table 6.1. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
00	Logic 0	0	0	0	0	0	0
01	Logic 1	0	0	0	0	0	1
02	MF0(2-bit LUT0/DFF0/LATCH0) OUT / Q/nQ	0	0	0	0	1	0
03	MF1(2-bit LUT1/DFF1/LATCH1) OUT / Q/nQ	0	0	0	0	1	1
04	MF2(2-bit LUT2/DFF2/LATCH2) OUT / Q/nQ	0	0	0	1	0	0
05	MF2(16-bit PGEN) OUT	0	0	0	1	0	1
06	MF3(3-bit LUT0/DFF3/LATCH3) OUT / Q/nQ	0	0	0	1	1	0
07	MF4(3-bit LUT1/DFF4/LATCH4) OUT / Q/nQ	0	0	0	1	1	1
08	MF5(3-bit LUT2/DFF5/LATCH5) OUT / Q/nQ	0	0	1	0	0	0
09	MF6(3-bit LUT3/DFF6/LATCH6) OUT / Q/nQ	0	0	1	0	0	1
10	MF7(3-bit LUT4/DFF7/LATCH7) OUT / Q/nQ	0	0	1	0	1	0
11	MF8(3-bit LUT5/DFF8/LATCH8) OUT / Q/nQ	0	0	1	0	1	1
12	MF9(3-bit LUT6/DFF9/LATCH9) OUT / Q/nQ	0	0	1	1	0	0
13	MF10(3-bit LUT7/DFF10/LATCH10) OUT / Q/nQ	0	0	1	1	0	1
14	MF11(3-bit LUT8/DFF11/LATCH11) OUT / Q/nQ	0	0	1	1	1	0
15	MF12(3-bit LUT9/DFF12/LATCH12) OUT / Q/nQ	0	0	1	1	1	1
16	MF13(3-bit LUT10/DFF13/LATCH13/8-bit PGEN0) OUT /Q/nQ	0	1	0	0	0	0
17	MF14(3-bit LUT11/DFF14/LATCH14/8-bit PGEN1) OUT /Q/nQ	0	1	0	0	0	1
18	MF15(3-bit LUT12/Shift Register) OUT0	0	1	0	0	1	0
19	MF15(3-bit LUT12/Shift Register) OUT1/nOUT1	0	1	0	0	1	1
20	MF15(3-bit LUT12/Shift Register) OUT2(LUT)/Q(1)	0	1	0	1	0	0
21	MF16(3-bit LUT13/8-bit TMR0) OUT	0	1	0	1	0	1
22	MF17(3-bit LUT14/8-bit TMR1) OUT	0	1	0	1	1	0
23	MF18(3-bit LUT15/8-bit TMR2) OUT	0	1	0	1	1	1
24	MF19(3-bit LUT16/8-bit TMR3) OUT	0	1	1	0	0	0
25	MF20(3-bit LUT17/8-bit TMR4) OUT	0	1	1	0	0	1
26	MF21(3-bit LUT18/8-bit TMR5) OUT	0	1	1	0	1	0
27	MF22(4-bit LUT0/16-bit TMR6(WS)) OUT	0	1	1	0	1	1
28	MF23(4-bit LUT1/16-bit TMR7) OUT	0	1	1	1	0	0
29	OSC0 OUT0	0	1	1	1	0	1
30	OSC0 OUT1	0	1	1	1	1	0
31	OSC1 OUT	0	1	1	1	1	1
32	MF24(4-bit LUT2/16-bit RPGEN) OUT	1	0	0	0	0	0
33	MF25(PDLY/Edge Detector) OUT/nOUT	1	0	0	0	0	1
34	Reserved	1	0	0	0	1	0
35	Reserved	1	0	0	0	1	1
36	Reserved	1	0	0	1	0	0
37	Reserved	1	0	0	1	0	1
38	Reserved	1	0	0	1	1	0
39	Reserved	1	0	0	1	1	1
40	Reserved	1	0	1	0	0	0
41	Reserved	1	0	1	0	0	1
42	Ready	1	0	1	0	1	0
43	ACMP0 OUT	1	0	1	0	1	1
44	ACMP1 OUT	1	0	1	1	0	0
45	ACMP2 OUT	1	0	1	1	0	1
46	ACMP3 OUT	1	0	1	1	1	0
47	Reserved	1	0	1	1	1	1
48	IO3 DOUT	1	1	0	0	0	0
49	IO2 DOUT	1	1	0	0	0	1
50	IO12 DOUT	1	1	0	0	1	0
51	IO5 DOUT	1	1	0	0	1	1
52	IO6 DOUT	1	1	0	1	0	0
53	IO7 DOUT	1	1	0	1	0	1
54	Reserved	1	1	0	1	1	0
55	IO8 DOUT	1	1	0	1	1	1

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
56	IO10 DOUT	1	1	1	0	0	0
57	IO11 DOUT	1	1	1	0	0	1
58	IO4 DOUT	1	1	1	0	1	0
59	Reserved	1	1	1	0	1	1
60	IO13 DOUT	1	1	1	1	0	0
61	IO14 DOUT	1	1	1	1	0	1
62	Reserved	1	1	1	1	1	0

6.3. Matrix Output

Table 6.2. Matrix Output Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
Connection matrix outputs				
0x2000	<5:0>	CMO0	MF0_2BLUT0_DFF0_IN0_CLK	MF0(2-bit LUT0/DFF0/LATCH0) IN0/CLK/nL
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7>			Reserved
0x2001	<5:0>	CMO1	MF0_2BLUT0_DFF0_IN1_D	MF0(2-bit LUT0/DFF0/LATCH0) IN1/D
	<7:6>			Reserved
0x2002	<5:0>	CMO2	MF1_2BLUT1_DFF1_IN0_CLK	MF1(2-bit LUT1/DFF1/LATCH1) IN0/CLK/nL
	<7:6>			Reserved
0x2003	<5:0>	CMO3	MF1_2BLUT1_DFF1_IN1_D	MF1(2-bit LUT1/DFF1/LATCH1) IN1/D
	<7:6>			Reserved
0x2004	<5:0>	CMO4	MF2_2BLUT2_DFF2_IN0_CLK	MF2(2-bit LUT2/DFF2/LATCH2) IN0/CLK/nL
	<7:6>			Reserved
0x2005	<5:0>	CMO5	MF2_2BLUT2_DFF2_IN1_D	MF2(2-bit LUT2/DFF2/LATCH2) IN1/D
	<7:6>			Reserved
0x2006	<5:0>	CMO6	MF2_16BPGEN0_IN0_CLK	MF2(16-bit PGEN) IN0/CLK
	<7:6>			Reserved
0x2007	<5:0>	CMO7	MF2_16BPGEN0_IN1_nRST	MF2(16-bit PGEN) IN1/nRST
	<7:6>			Reserved
0x2008	<5:0>	CMO8	MF3_3BLUT0_DFF3_IN0_CLK	MF3(3-bit LUT0/DFF3/LATCH3) IN0/CLK/nL
	<7:6>			Reserved
0x2009	<5:0>	CMO9	MF3_3BLUT0_DFF3_IN1_D	MF3(3-bit LUT0/DFF3/LATCH3) IN1/D
	<7:6>			Reserved
0x200A	<5:0>	CMO10	MF3_3BLUT0_DFF3_IN2_RST	MF3(3-bit LUT0/DFF3/LATCH3) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x200B	<5:0>	CMO11	MF4_3BLUT1_DFF4_IN0_CLK	MF4(3-bit LUT1/DFF4/LATCH4) IN0/CLK/nL
	<7:6>			Reserved
0x200C	<5:0>	CMO12	MF4_3BLUT1_DFF4_IN1_D	MF4(3-bit LUT1/DFF4/LATCH4) IN1/D
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
0x200D	<5:0>	CMO13	MF4_3BLUT1_DFF4_IN2_RST	MF4(3-bit LUT1/DFF4/LATCH4) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x200E	<5:0>	CMO14	MF5_3BLUT2_DFF5_IN0_CLK	MF5(3-bit LUT2/DFF5/LATCH5) IN0/CLK/nL

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<7:6>			Reserved
0x200F	<5:0>	CMO15	MF5_3BLUT2_DFF5_IN1_D	MF5(3-bit LUT2/DFF5/LATCH5) IN1/D
	<7:6>			Reserved
0x2010	<5:0>	CMO16	MF5_3BLUT2_DFF5_IN2_RST	MF5(3-bit LUT2/DFF5/LATCH5) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x2011	<5:0>	CMO17	MF6_3BLUT3_DFF6_IN0_CLK	MF6(3-bit LUT3/DFF6/LATCH6) IN0/CLK/nL
	<7:6>			Reserved
0x2012	<5:0>	CMO18	MF6_3BLUT3_DFF6_IN1_D	MF6(3-bit LUT3/DFF6/LATCH6) IN1/D
	<7:6>			Reserved
0x2013	<5:0>	CMO19	MF6_3BLUT3_DFF6_IN2_RST	MF6(3-bit LUT3/DFF6/LATCH6) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x2014	<5:0>	CMO20	MF7_3BLUT4_DFF7_IN0_CLK	MF7(3-bit LUT4/DFF7/LATCH7) IN0/CLK/nL
	<7:6>			Reserved
0x2015	<5:0>	CMO21	MF7_3BLUT4_DFF7_IN1_D	MF7(3-bit LUT4/DFF7/LATCH7) IN1/D
	<7:6>			Reserved
0x2016	<5:0>	CMO22	MF7_3BLUT4_DFF7_IN2_RST	MF7(3-bit LUT4/DFF7/LATCH7) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x2017	<5:0>	CMO23	MF8_3BLUT5_DFF8_IN0_CLK	MF8(3-bit LUT5/DFF8/LATCH8) IN0/CLK/nL
	<7:6>			Reserved
0x2018	<5:0>	CMO24	MF8_3BLUT5_DFF8_IN1_D	MF8(3-bit LUT5/DFF8/LATCH8) IN1/D
	<7:6>			Reserved
0x2019	<5:0>	CMO25	MF8_3BLUT5_DFF8_IN2_RST	MF8(3-bit LUT5/DFF8/LATCH8) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x201A	<5:0>	CMO26	MF9_3BLUT6_DFF9_IN0_CLK	MF9(3-bit LUT6/DFF9/LATCH9) IN0/CLK/nL
	<7:6>			Reserved
0x201B	<5:0>	CMO27	MF9_3BLUT6_DFF9_IN1_D	MF9(3-bit LUT6/DFF9/LATCH9) IN1/D
	<6>			Reserved
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
0x201C	<5:0>	CMO28	MF9_3BLUT6_DFF9_IN2_RST	MF9(3-bit LUT6/DFF9/LATCH9) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x201D	<5:0>	CMO29	MF10_3BLUT7_DFF10_IN0_CLK	MF10(3-bit LUT7/DFF10/LATCH10) IN0/CLK/nL
	<7:6>			Reserved
0x201E	<5:0>	CMO30	MF10_3BLUT7_DFF10_IN1_D	MF10(3-bit LUT7/DFF10/LATCH10) IN1/D
	<7:6>			Reserved
0x201F	<5:0>	CMO31	MF10_3BLUT7_DFF10_IN2_RST	MF10(3-bit LUT7/DFF10/LATCH10) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x2020	<5:0>	CMO32	MF11_3BLUT8_DFF11_IN0_CLK	MF11(3-bit LUT8/DFF11/LATCH11) IN0/CLK/nL
	<7:6>			Reserved
0x2021	<5:0>	CMO33	MF11_3BLUT8_DFF11_IN1_D	MF11(3-bit LUT8/DFF11/LATCH11) IN1/D
	<7:6>			Reserved
0x2022	<5:0>	CMO34	MF11_3BLUT8_DFF11_IN2_RST	MF11(3-bit LUT8/DFF11/LATCH11) IN2/(n)RST/(n)SET
	<7:6>			Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
0x2023	<5:0>	CMO35	MF12_3BLUT9_DFF12_IN0_CLK	MF12(3-bit LUT9/DFF12/LATCH12) IN0/CLK/nL
	<7:6>			Reserved
0x2024	<5:0>	CMO36	MF12_3BLUT9_DFF12_IN1_D	MF12(3-bit LUT9/DFF12/LATCH12) IN1/D
	<7:6>			Reserved
0x2025	<5:0>	CMO37	MF12_3BLUT9_DFF12_IN2_RST	MF12(3-bit LUT9/DFF12/LATCH12) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x2026	<5:0>	CMO38	MF13_3BLUT10_DFF13_8BPGEN0_IN0_CLK	MF13(3-bit LUT10/DFF13/LATCH13/8-bit PGEN0) IN0/CLK/nL
	<7:6>			Reserved
0x2027	<5:0	CMO39	MF13_3BLUT10_DFF13_8BPGEN0_IN1_D_KEEP	MF13(3-bit LUT10/DFF13/LATCH13/8-bit PGEN0) IN1/D/KEEP
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7>			Reserved
0x2028	<5:0>	CMO40	MF13_3BLUT10_DFF13_8BPGEN0_IN2_RST	MF13(3-bit LUT10/DFF13/LATCH13/8-bit PGEN0) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x2029	<5:0>	CMO41	MF14_3BLUT11_DFF14_8BPGEN1_IN0_CLK	MF14(3-bit LUT11/DFF14/LATCH14/8-bit PGEN1) IN0/CLK/nL
	<7:6>			Reserved
0x202A	<5:0>	CMO42	MF14_3BLUT11_DFF14_8BPGEN1_IN1_D_KEEP	MF14(3-bit LUT11/DFF14/LATCH14/8-bit PGEN1) IN1/D/KEEP
	<7:6>			Reserved
0x202B	<5:0>	CMO43	MF14_3BLUT11_DFF14_8BPGEN1_IN2_RST	MF14(3-bit LUT11/DFF14/LATCH14/8-bit PGEN1) IN2/(n)RST/(n)SET
	<7:6>			Reserved
0x202C	<5:0>	CMO44	MF15_3BLUT12_SH_REG_IN0_CLK	MF15(3-bit LUT12/Shift Register) IN0/CLK
	<7:6>			Reserved
0x202D	<5:0>	CMO45	MF15_3BLUT12_SH_REG_IN1_D	MF15(3-bit LUT12/Shift Register) IN1/D
	<7:6>			Reserved
0x202E	<5:0>	CMO46	MF15_3BLUT12_SH_REG_IN2_nRST	MF15(3-bit LUT12/Shift Register) IN2/nRST
	<7:6>			Reserved
0x202F	<5:0>	CMO47	MF16_3BLUT13_8BTMR0_IN0_CLK	MF16(3-bit LUT13/8-bit TMR0) IN0/CLK
	<7:6>			Reserved
0x2030	<5:0>	CMO48	MF16_3BLUT13_8BTMR0_IN1_RST	MF16(3-bit LUT13/8-bit TMR0) IN1/IN/RST
	<7:6>			Reserved
0x2031	<5:0>	CMO49	MF16_3BLUT13_8BTMR0_IN2_KEEP	MF16(3-bit LUT13/8-bit TMR0) IN2/KEEP
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7>			Reserved
0x2032	<5:0>	CMO50	MF17_3BLUT14_8BTMR1_IN0_CLK	MF17(3-bit LUT14/8-bit TMR1) IN0/CLK
	<7:6>			Reserved
0x2033	<5:0>	CMO51	MF17_3BLUT14_8BTMR1_IN1_RST	MF17(3-bit LUT14/8-bit TMR1) IN1/IN/RST
	<7:6>			Reserved
0x2034	<5:0>	CMO52	MF17_3BLUT14_8BTMR1_IN2_KEEP	MF17(3-bit LUT14/8-bit TMR1) IN2/KEEP
	<7:6>			Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
0x2035	<5:0>	CMO53	MF18_3BLUT15_8BTMR2_IN0_CLK	MF18(3-bit LUT15/8-bit TMR2) IN0/CLK
	<7:6>			Reserved
0x2036	<5:0>	CMO54	MF18_3BLUT15_8BTMR2_IN1_RST	MF18(3-bit LUT15/8-bit TMR2) IN1/IN/RST
	<7:6>			Reserved
0x2037	<5:0>	CMO55	MF18_3BLUT15_8BTMR2_IN2_KEEP	MF18(3-bit LUT15/8-bit TMR2) IN2/KEEP
	<6>			Reserved
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
0x2038	<5:0>	CMO56	MF19_3BLUT16_8BTMR3_IN0_CLK	MF19(3-bit LUT16/8-bit TMR3) IN0/CLK
	<7:6>			Reserved
0x2039	<5:0>	CMO57	MF19_3BLUT16_8BTMR3_IN1_RST	MF19(3-bit LUT16/8-bit TMR3) IN1/IN/RST
	<7:6>			Reserved
0x203A	<5:0>	CMO58	MF19_3BLUT16_8BTMR3_IN2_KEEP	MF19(3-bit LUT16/8-bit TMR3) IN2/KEEP
	<7:6>			Reserved
0x203B	<5:0>	CMO59	MF20_3BLUT17_8BTMR4_IN0_CLK	MF20(3-bit LUT17/8-bit TMR4) IN0/CLK
	<7:6>			Reserved
0x203C	<5:0>	CMO60	MF20_3BLUT17_8BTMR4_IN1_RST	MF20(3-bit LUT17/8-bit TMR4) IN1/IN/RST
	<7:6>			Reserved
0x203D	<5:0>	CMO61	MF20_3BLUT17_8BTMR4_IN2_KEEP	MF20(3-bit LUT17/8-bit TMR4) IN2/KEEP
	<7:6>			Reserved
0x203E	<5:0>	CMO62	MF21_3BLUT18_8BTMR5_IN0_CLK	MF21(3-bit LUT18/8-bit TMR5) IN0/CLK
	<7:6>			Reserved
0x203F	<5:0>	CMO63	MF21_3BLUT18_8BTMR5_IN1_RST	MF21(3-bit LUT18/8-bit TMR5) IN1/IN/RST
	<7:6>			Reserved
0x2040	<5:0>	CMO64	MF21_3BLUT18_8BTMR5_IN2_KEEP	MF21(3-bit LUT18/8-bit TMR5) IN2/KEEP
	<7:6>			Reserved
0x2041	<5:0>	CMO65	MF22_4BLUT0_16BTMR6_IN0_CLK	MF22(4-bit LUT0/16-bit TMR6(WS)) IN0/CLK
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7>			Reserved
0x2042	<5:0>	CMO66	MF22_4BLUT0_16BTMR6_IN1_RST	MF22(4-bit LUT0/16-bit TMR6(WS)) IN1/IN/RST
	<7:6>			Reserved
0x2043	<5:0>	CMO67	MF22_4BLUT0_16BTMR6_IN2_KEEP	MF22(4-bit LUT0/16-bit TMR6(WS)) IN2/KEEP
	<7:6>			Reserved
0x2044	<5:0>	CMO68	MF22_4BLUT0_16BTMR6_IN3_UP	MF22(4-bit LUT0/16-bit TMR6(WS)) IN3/UP
	<7:6>			Reserved
0x2045	<5:0>	CMO69	MF23_4BLUT1_16BTMR7_IN0_CLK	MF23(4-bit LUT1/16-bit TMR7) IN0/CLK
	<7:6>			Reserved
0x2046	<5:0>	CMO70	MF23_4BLUT1_16BTMR7_IN1_RST	MF23(4-bit LUT1/16-bit TMR7) IN1/IN/RST
	<7:6>			Reserved

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
0x2047	<5:0>	CMO71	MF23_4BLUT1_16BTMR7_IN2_KEEP	MF23(4-bit LUT1/16-bit TMR7) IN2/KEEP
	<7:6>			Reserved
0x2048	<5:0>	CMO72	MF23_4BLUT1_16BTMR7_IN3_UP	MF23(4-bit LUT1/16-bit TMR7) IN3/UP
	<7:6>			Reserved
0x2049	<5:0>	CMO73	MF24_4BLUT2_16BRPGEN_IN0_CLK	MF24(4-bit LUT2/16-bit RPGEN) IN0/CLK
	<7:6>			Reserved
0x204A	<5:0>	CMO74	MF24_4BLUT2_16BRPGEN_IN1_RST	MF24(4-bit LUT2/16-bit RPGEN) IN1/nRST
	<6>			Reserved
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
0x204B	<5:0>	CMO75	MF24_4BLUT2_16BRPGEN_IN2_KEEP	MF24(4-bit LUT2/16-bit RPGEN) IN2/KEEP
	<7:6>			Reserved
0x204C	<5:0>	CMO76	MF24_4BLUT2_16BRPGEN_IN3_REV	MF24(4-bit LUT2/16-bit RPGEN) IN3/REV
	<7:6>			Reserved
0x204D	<5:0>	CMO77	MF25_PDLY_ED_IN	MF25(PDLY/Edge Detector) IN
	<7:6>			Reserved
0x204E	<7:0>	CMO78		Reserve
0x204F	<5:0>	CMO79	OSC0_CTRL_IN	OSC0 CTRL IN
	<7:6>			Reserved
0x2050	<5:0>	CMO80	OSC1_CTRL_IN	OSC1 CTRL IN
	<7:6>			Reserved
0x2051	<5:0>	CMO81	ACMP0_PWR_ON	ACMP0 PWR ON
	<7:6>			Reserved
0x2052	<5:0>	CMO82	ACMP1_PWR_ON	ACMP1 PWR ON
	<7:6>			Reserved
0x2053	<5:0>	CMO83	ACMP2_PWR_ON	ACMP2 PWR ON
	<7:6>			Reserved
0x2054	<5:0>	CMO84	ACMP3_PWR_ON	ACMP3 PWR ON
	<7:6>			Reserved
0x2055	<5:0>	CMO85	IO3_DIN	IO3 DIN
	<6>			Reserved
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
0x2057	<5:0>	CMO87	IO2_DIN	IO2 DIN
	<7:6>			Reserved
0x2058	<5:0>	CMO88	IO12_DIN	IO12 DIN
	<7:6>			Reserved
0x2059	<5:0>	CMO89	IO12_DIR_VREF_TS_PWR_ON	IO12 DIR shared with Voltage reference (VREF) PWR_ON and Temperature sensor (TS) PWR_ON
	<7:6>			Reserved
0x205A	<5:0>	CMO90	IO5_DIN	IO5 DIN
	<7:6>			Reserved
0x205B	<5:0>	CMO91	IO6_DIN	IO6 DIN
	<7:6>			Reserved
0x205C	<5:0>	CMO92	IO6_DIR	IO6 DIR
	<7:6>			Reserved
0x205D	<7:0>	CMO93		Reserved
0x205E	<7:0>	CMO94		Reserved
0x205F	<5:0>	CMO95	IO7_DIN	IO7 DIN
	<7:6>			Reserved
0x2060	<5:0>	CMO96	IO7_DIR	IO7 DIR

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7>			Reserved
0x2061	<7:0>	CMO97		Reserved
0x2063	<7:0>	CMO99		Reserved
0x2064	<5:0>	CMO100	IO10_DIN	IO10 DIN
	<7:6>			Reserved
0x2065	<5:0>	CMO101	IO10_DIR	IO10 DIR
	<7:6>			Reserved
0x2066	<5:0>	CMO102	IO11_DIN	IO11 DIN
	<7:6>			Reserved
0x2067	<5:0>	CMO103	IO4_DIN	IO4 DIN
	<7:6>			Reserved
0x2068	<5:0>	CMO104	IO4_DIR	IO4 DIR
	<7:6>			Reserved
0x2069	<7:0>	CMO105		Reserved
0x206A	<5:0>	CMO106	IO13_DIN	IO13 DIN
	<7:6>			Reserved
0x206B	<5:0>	CMO107	IO13_DIR	IO13 DIR
	<7:6>			Reserved
0x206C	<5:0>	CMO108	IO14_DIN	IO14 DIN
	<7:6>			Reserved
0x206D	<5:0>	CMO109	IO14_DIR	IO14 DIR
	<7:6>			Reserved
0x206E	<7:0>	CMO110		Reserved

7. Multifunctional Macrocells

The AM1U1514 contains 26 multifunction macrocells (MF), each configurable to perform one of several logic or timing functions: Look-Up Tables (LUT), D flip-flops (DFF), latches, timers, pattern generators, shift register, programmable delay, and edge detectors:

- Two selectable 2-bit LUTs or DFF/LATCHs;
- One selectable 2-bit LUT or DFF/LATCH or 16-bit Pattern Generator;
- Ten selectable 3-bit LUTs or DFF/LATCHs;
- Two selectable 3-bit LUTs or 8-bit Pattern Generators
- One selectable 3-bit LUT or 16-bit Shift Register;
- Six Selectable 3-bit LUTs or 8-bit Timers (TMR);
- Two Selectable 4-bit LUTs or 16-bit Timers;
- One Selectable 4-bit LUT or 16-bit Reversible Pattern Generator;
- One Programmable Delay or Edge Detector.

7.1. MF (2-bit LUT/DFF/LATCH) Macrocells

The AM1U1514 has MF macrocells capable of serving as either 2-bit LUTs, DFFs or LATCHs (see Figure 7.1).

When the MF macrocells are used as LUT, the 2-bit LUT takes two input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.1.

When the macrocells are used as DFF or LATCH, the two input signals from the connection matrix go to the data (D) and clock/nlatch (CLK/nL) inputs for the DFF/LATCH, and the output goes back to the connection matrix. Operation of the DFF and LATCH are shown in the Table 7.2, Table 7.3.

Table 7.1. 2-bit LUT Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0

Table 7.2. Operation of the DFF

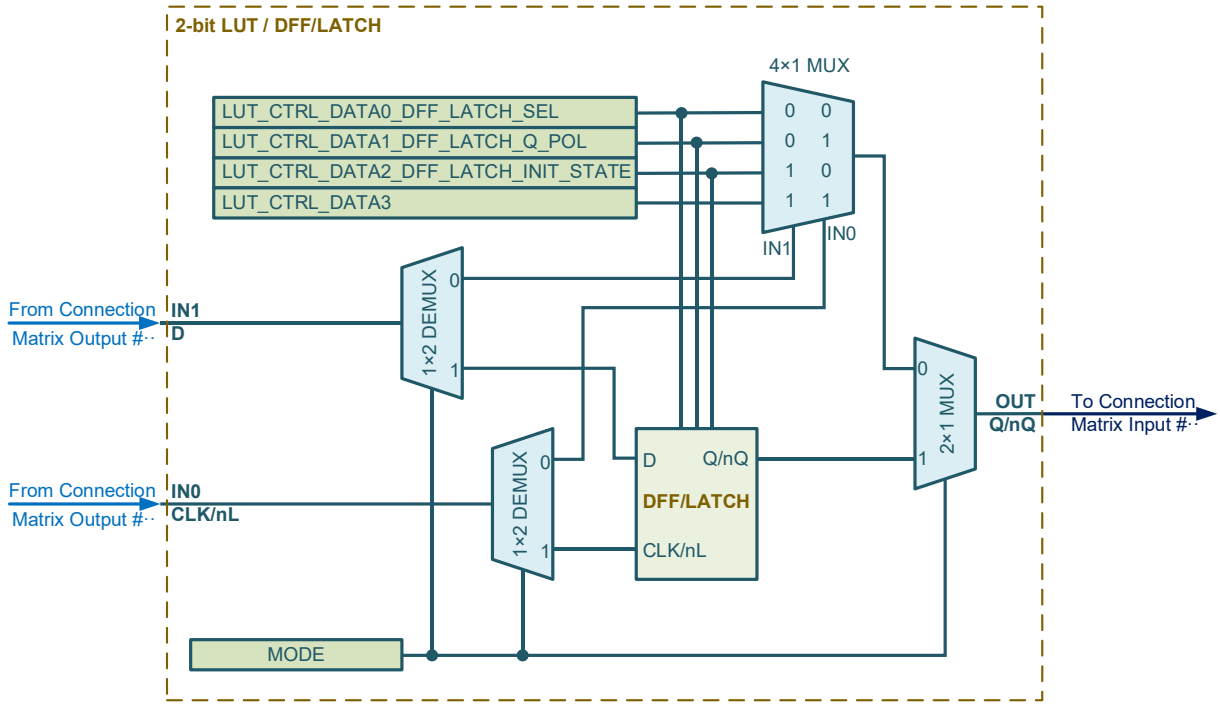
D	CLK	Q(t)/nQ(t)
0	↓	0/1
0	↑	t–1
1	↓	1/0
1	↑	t–1

Note 7.1: X – Don't Care
Note 7.2: t–1 – Previous State

Table 7.3. Operation of the LATCH

nL	D	Q(t)/nQ(t)
0	0	t–1
0	1	t–1
1	0	0/1
1	1	1/0

Note 7.3: X – Don't Care
Note 7.4: t–1 – Previous State



MF#	IN0/CLK/nL	IN1/D	OUT/Q/nQ
MF0 (2-bit LUT0/DFF0/LATCH0)	CMO0	CMO1	CMI2
MF1 (2-bit LUT1/DFF1/LATCH1)	CMO2	CMO3	CMI3

Figure 7.1. Schematic diagram of MF (2-bit LUT/DFF/LATCH)

7.1.1. MF0 (2-bit LUT0/DFF0/LATCH0) Macrocell

MF0 registers are listed in Table 7.4.

Table 7.4. MF0(2-bit LUT0/DFF0/LATCH0) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF0 (2-bit LUT0/DFF0/LATCH0)				
0x5000	<0>	MF0_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<2>		LUT_CTRL_DATA2_DFF_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.5): 0: LOW 1: HIGH
	<3>		LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
	<4>		MODE	MF mode: 0: LUT 1: DFF/LATCH
	<7:5>			Reserved

Note 7.5: In Latch mode, initial state is always High; this bit has no effect.

The MF0 (2-bit LUT0/DFF0/LATCH0) macrocell, if programmed for a LUT function, uses 4 bits to define its output function by MF0_CONF<3:0> (see Table 7.5).

Table 7.5. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	MF0_CONF<0>	LSB
0	1	MF0_CONF<1>	
1	0	MF0_CONF<2>	
1	1	MF0_CONF<3>	MSB

7.1.2. MF1 (2-bit LUT1/DFF1/LATCH1) Macrocell

MF1 registers are listed in Table 7.6.

Table 7.6. 2-bit LUT1/DFF1/LATCH1 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF1 (2-bit LUT1/DFF1/LATCH1)				
0x5100	<0>	MF1_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.6): 0: LOW 1: HIGH

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<3>		LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
	<4>		MODE	MF mode: 0: LUT 1: DFF/LATCH
	<7:5>			Reserved

Note 7.6: In Latch mode, initial state is always High; this bit has no effect.

The MF1 (2-bit LUT1/DFF1/LATCH1) macrocell, if programmed for a LUT function, uses 4 bits to define its output function by MF1_CONF<3:0> (see Table 7.7).

Table 7.7. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	MF1_CONF<0>	LSB
0	1	MF1_CONF<1>	
1	0	MF1_CONF<2>	
1	1	MF1_CONF<3>	MSB

7.2. MF (2-bit LUT/DFF/LATCH/16-bit PGEN) Macrocell

The AM1U1514 has a MF macrocell that can serve as a logic or timing function. This MF macrocell can serve as a Look Up Table (LUT), DFF, LATCH, or Programmable Pattern Generator (PGEN).

When the MF macrocell is used as LUT, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.8.

When the macrocells are used as DFF or LATCH, the two input signals from the connection matrix go to the data (D) and clock/nlatch (CLK/nL) inputs for the DFF/LATCH, and the output goes back to the connection matrix. Operation of the DFF and LATCH are shown in the Table 7.9, Table 7.10.

When the MF macrocell is used as a Programmable Pattern Generator (PGEN), the macrocell outputs configurable pattern by the input clock (CLK) signal. The length of the pattern is configurable and can be selected from 2 to 16 bits. See Figure 7.2 and Figure 7.3 and Table 7.11.

Table 7.8. 2-bit LUT Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0

Table 7.9. Operation of the DFF

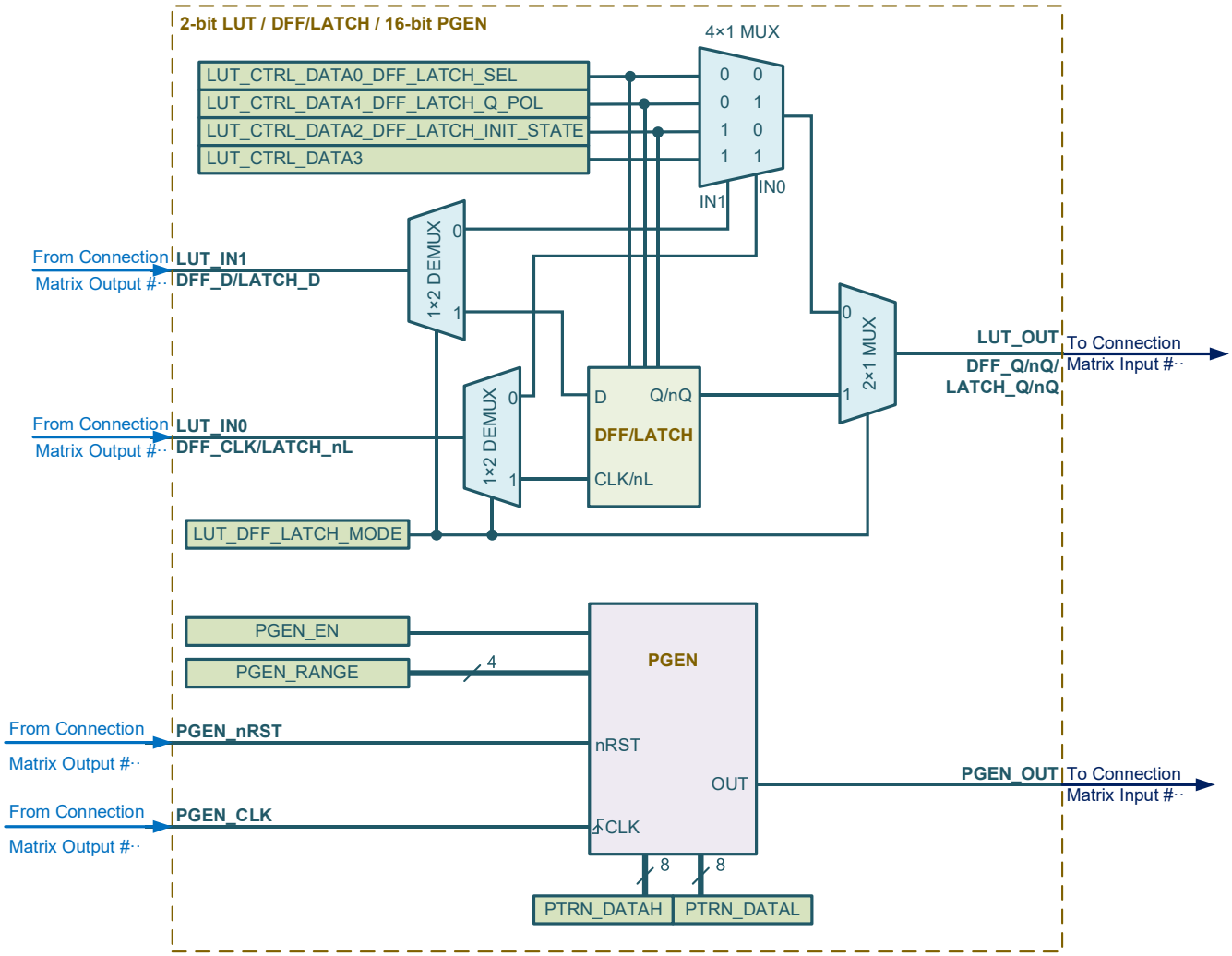
D	CLK	Q(t)/nQ(t)
0	⤴	0/1
0	⤵	t–1
1	⤴	1/0
1	⤵	t–1

Note 7.7: X – Don't Care
Note 7.8: t–1 – Previous State

Table 7.10. Operation of the LATCH

nL	D	Q(t)/nQ(t)
0	0	t–1
0	1	t–1
1	0	0/1
1	1	1/0

Note 7.9: X – Don't Care
Note 7.10: t–1 – Previous State



MF#	LUT_IN0 DFF_CLK LATCH_nL	LUT_IN1 DFF_D LATCH_D	PGEN_CLK	PGEN_nRST	LUT_OUT DFF_Q/nQ LATCH_Q/nQ	PGEN_OUT
MF2(2-bit LUT2 / DFF2 / LATCH2 / 16-bit PGEN)	CMO4	CMO5	CMO6	CMO7	CMI4	CMI5

Figure 7.2. Schematic diagram of MF3 (2-bit LUT2/DFF2/LATCH2/16-bit PGEN)

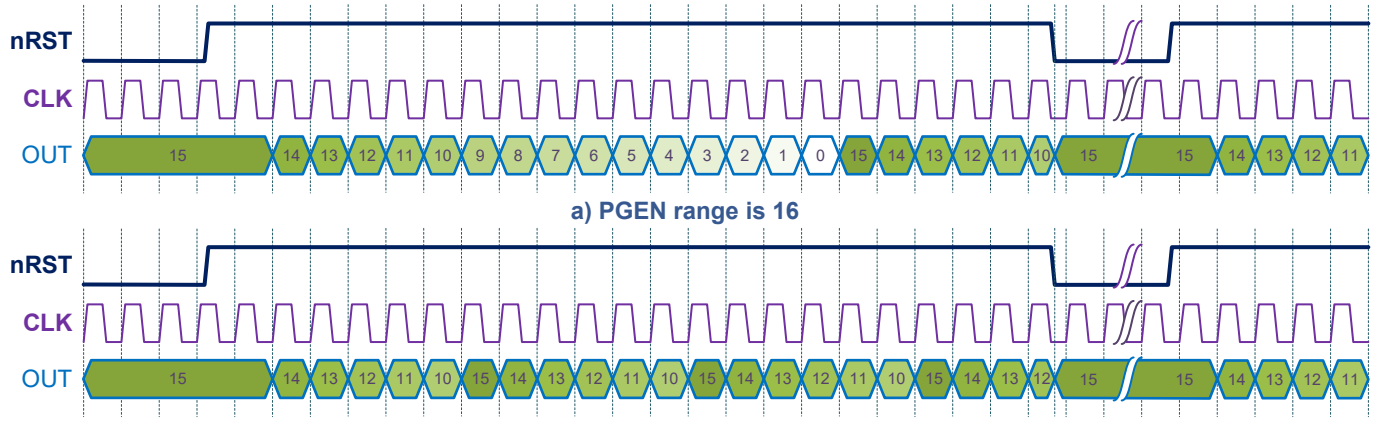


Figure 7.3. Pattern Generator Timing Diagram

7.2.1. MF2 (2-bit LUT2/DFF2/LATCH2/16-bit PGEN) Macrocells

Table 7.11. MF2 (2-bit LUT2/DFF2/LATCH2/16-bit PGEN) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF3 (2-bit LUT2/DFF2/LATCH2/16-bit PGEN)				
0x5200	<0>	MF2_CONF0	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
	<3>		LUT_CTRL_DATA3	3rd bit of LUT control data: 0: LOW 1: HIGH
	<4>		LUT_DFF_LATCH_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<5>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7:6>			Reserved
0x5300	<3:0>	MF2_CONF1	PGEN_RANGE	PGEN range
	<4>		PGEN_EN	PGEN: 0: Disable 1: Enable
	<7:5>			Reserved
0x5301	<7:0>	MF2_PTRN_DATAL		Low byte of pattern data
0x5302	<7:0>	MF2_PTRN_DATAH		High byte of pattern data

The 2-bit LUT2 uses 4 bits to define its output function by MF2_CONF0<3:0> (see Table 7.12).

Table 7.12. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	MF2_CONF0<0>	LSB
0	1	MF2_CONF0<1>	
1	0	MF2_CONF0<2>	
1	1	MF2_CONF0<3>	MSB

The Pattern Generator uses 4 bits to define its bit range and 2 bytes to define Pattern Data (see Table 7.13).

Table 7.13. 16-bit Pattern Generator Registers

Function	Register Bit Address	Register Definition
PGEN range	MF2_CONF1<3:0>	4-bit data
PGEN pattern data	MF2_PTRN_DATAL<7:0>	16-bit data
	MF2_PTRN_DATAH<7:0>	

7.3. MF (3-bit LUT/DFF/LATCH) Macrocells

The AM1U1514 has a MF macrocell that can serve as either 3-bit LUTs or as DFF/LATCHs (Figure 7.4). The mode of each macrocell is set corresponding register (see Table 7.17).

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.14.

When the macrocells are used as DFF or LATCH, the three input signals from the connection matrix go to the data (D), clock/nlatch (CLK/nL) and (n)RST/(n)SET inputs of the DFF/LATCH, and the output goes back to the connection matrix. Operation of the DFF and LATCH are shown in the Table 7.15, Table 7.16.

Table 7.14. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

Table 7.15. Operation of the DFF

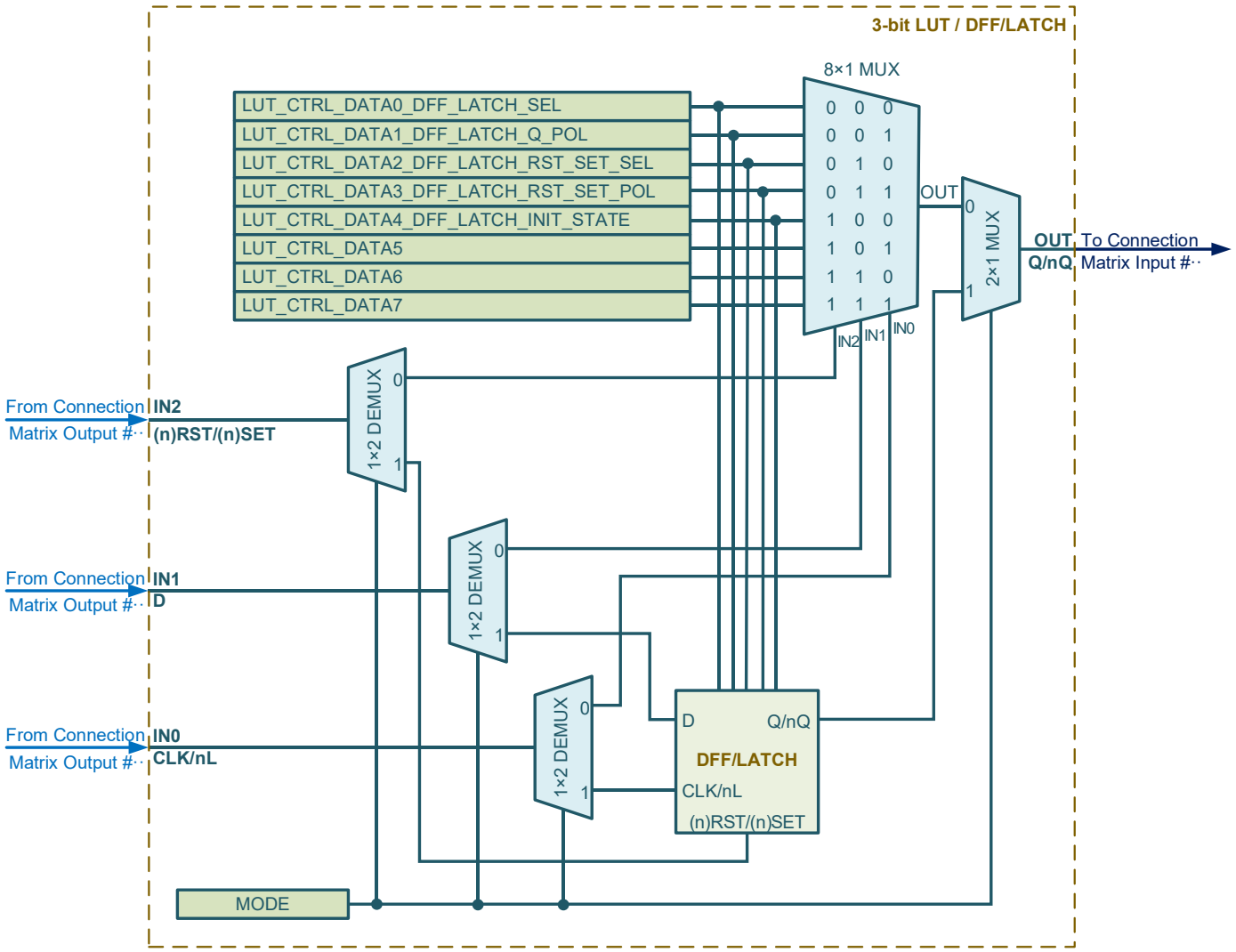
nRST/nSET	D	CLK	Q(t)/nQ(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	⤓	0/1
1	0	⤒	t–1
1	1	⤓	1/0
1	1	⤒	t–1

Note 7.11: X – Don't Care
Note 7.12: t–1 – Previous State

Table 7.16. Operation of the LATCH

nSET	nL	D	Q(t)/nQ(t)
nSET = 0	X	X	1/0
1	0	0	t–1
1	0	1	t–1
1	1	0	0/1
1	1	1	1/0

Note 7.13: X – Don't Care
Note 7.14: t–1 – Previous State



MF#	IN0/CLK/nL	IN1/D	IN2/(n)RST/(n)SET	OUT/Q/nQ
MF3 (3-bit LUT0/DFF3/LATCH3)	CMO8	CMO9	CMO10	CMI6
MF4 (3-bit LUT1/DFF4/LATCH4)	CMO11	CMO12	CMO13	CMI7
MF5 (3-bit LUT2/DFF5/LATCH5)	CMO14	CMO15	CMO16	CMI8
MF6 (3-bit LUT3/DFF6/LATCH6)	CMO17	CMO18	CMO19	CMI9
MF7 (3-bit LUT4/DFF7/LATCH7)	CMO20	CMO21	CMO22	CMI10
MF8 (3-bit LUT5/DFF8/LATCH8)	CMO23	CMO24	CMO25	CMI11
MF9 (3-bit LUT6/DFF9/LATCH9)	CMO26	CMO27	CMO28	CMI12
MF10 (3-bit LUT7/DFF10/LATCH10)	CMO29	CMO30	CMO31	CMI13
MF11 (3-bit LUT8/DFF11/LATCH11)	CMO32	CMO33	CMO34	CMI14
MF12 (3-bit LUT9/DFF12/LATCH12)	CMO35	CMO36	CMO37	CMI15

Figure 7.4. Schematic diagram of MF (3-bit LUT/DFF/LATCH)

Table 7.17. MF (3-bit LUT/DFF/LATCH) mode settings

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF4 (3-bit LUT0/DFF3/LATCH3)…MF13 (3-bit LUT9/DFF12/LATCH12)				
0x5400	<0>	MF3_10_MODE	MF3_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<1>		MF4_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<2>		MF5_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<3>		MF6_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<4>		MF7_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<5>		MF8_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<6>		MF9_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<7>		MF10_MODE	MF mode: 0: LUT 1: DFF/LATCH
0x5401	<0>	MF11_12_MODE	MF11_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<1>		MF12_MODE	MF mode: 0: LUT 1: DFF/LATCH
	<2>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7:3>			Reserved

7.3.1. MF3 (3-bit LUT0/DFF3/LATCH3)

MF3 registers are listed in Table 7.18.

Table 7.18. 3-bit LUT0/DFF3/LATCH3 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF3 (3-bit LUT0/DFF3/LATCH3)				
0x5500	<0>	MF3_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0^{th} bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1^{st} bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.15): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.16): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.15: Must be set to 1 in LATCH mode.
Note 7.16: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT0 uses 8-bit register to define its output function (see Table 7.19).

Table 7.19. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF3_CONF<0>	LSB
0	0	1	MF3_CONF<1>	
0	1	0	MF3_CONF<2>	
0	1	1	MF3_CONF<3>	
1	0	0	MF3_CONF<4>	
1	0	1	MF3_CONF<5>	
1	1	0	MF3_CONF<6>	
1	1	1	MF3_CONF<7>	MSB

7.3.2. MF4 (3-bit LUT1/DFF4/LATCH4)

MF4 registers are listed in Table 7.20.

Table 7.20. MF4 (3-bit LUT1/DFF4/LATCH4) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF4 (3-bit LUT1/DFF4/LATCH4)				
0x5600	<0>	MF4_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.17): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.18): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.17: Must be set to 1 in LATCH mode.

Note 7.18: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT1 uses 8-bit register to define its output function (see Table 7.21).

Table 7.21. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF4_CONF<0>	LSB
0	0	1	MF4_CONF<1>	
0	1	0	MF4_CONF<2>	
0	1	1	MF4_CONF<3>	
1	0	0	MF4_CONF<4>	
1	0	1	MF4_CONF<5>	
1	1	0	MF4_CONF<6>	
1	1	1	MF4_CONF<7>	MSB

7.3.3. MF5 (3-bit LUT2/DFF5/LATCH5)

MF5 registers are listed in Table 7.22.

Table 7.22. MF5(3-bit LUT2/DFF5/LATCH5) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF5 (3-bit LUT2/DFF5/LATCH5)				
0x5700	<0>	MF5_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.19): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.20): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.19: Must be set to 1 in LATCH mode.
Note 7.20: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT2 uses 8-bit register to define its output function (see Table 7.23).

Table 7.23. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF5_CONF<0>	LSB
0	0	1	MF5_CONF<1>	
0	1	0	MF5_CONF<2>	
0	1	1	MF5_CONF<3>	
1	0	0	MF5_CONF<4>	
1	0	1	MF5_CONF<5>	
1	1	0	MF5_CONF<6>	
1	1	1	MF5_CONF<7>	MSB

7.3.4. MF6 (3-bit LUT3/DFF6/LATCH6)

MF6 registers are listed in Table 7.24.

Table 7.24. MF6 (3-bit LUT3/DFF6/LATCH6) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF6 (3-bit LUT3/DFF6/LATCH6)				
0x5800	<0>	MF6_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.21): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.22): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.21: Must be set to 1 in LATCH mode.
Note 7.22: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT3 uses 8-bit register to define its output function (see Table 7.25).

Table 7.25. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF6_CONF<0>	LSB
0	0	1	MF6_CONF<1>	
0	1	0	MF6_CONF<2>	
0	1	1	MF6_CONF<3>	
1	0	0	MF6_CONF<4>	
1	0	1	MF6_CONF<5>	
1	1	0	MF6_CONF<6>	
1	1	1	MF6_CONF<7>	MSB

7.3.5. MF7 (3-bit LUT4/DFF7/LATCH7)

MF7 registers are listed in Table 7.26.

Table 7.26. MF7 (3-bit LUT4/DFF7/LATCH7) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF7 (3-bit LUT4/DFF7/LATCH7)				
0x5900	<0>	MF7_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.23): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.24): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.23: Must be set to 1 in LATCH mode.

Note 7.24: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT4 uses 8-bit register to define its output function (see Table 7.27).

Table 7.27. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF7_CONF<0>	LSB
0	0	1	MF7_CONF<1>	
0	1	0	MF7_CONF<2>	
0	1	1	MF7_CONF<3>	
1	0	0	MF7_CONF<4>	
1	0	1	MF7_CONF<5>	
1	1	0	MF7_CONF<6>	
1	1	1	MF7_CONF<7>	MSB

7.3.6. MF8 (3-bit LUT5/DFF8/LATCH8)

MF8 registers are listed in Table 7.28.

Table 7.28. MF8 (3-bit LUT5/DFF8/LATCH8) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF8 (3-bit LUT5/DFF8/LATCH8)				
0x5A00	<0>	MF8_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.25): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.23): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.25: Must be set to 1 in LATCH mode.

Note 7.26: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT5 uses 8-bit register to define its output function (see Table 7.29).

Table 7.29. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF8_CONF<0>	LSB
0	0	1	MF8_CONF<1>	
0	1	0	MF8_CONF<2>	
0	1	1	MF8_CONF<3>	
1	0	0	MF8_CONF<4>	
1	0	1	MF8_CONF<5>	
1	1	0	MF8_CONF<6>	
1	1	1	MF8_CONF<7>	MSB

7.3.7. MF9 (3-bit LUT6/DFF9/LATCH9)

MF9 registers are listed in Table 7.30.

Table 7.30. MF9 (3-bit LUT6/DFF9/LATCH9) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF9 (3-bit LUT6/DFF9/LATCH9)				
0x5B00	<0>	MF9_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.27): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.28): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.27: Must be set to 1 in LATCH mode.

Note 7.28: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT6 uses 8-bit register to define its output function (see Table 7.31).

Table 7.31. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF9_CONF<0>	LSB
0	0	1	MF9_CONF<1>	
0	1	0	MF9_CONF<2>	
0	1	1	MF9_CONF<3>	
1	0	0	MF9_CONF<4>	
1	0	1	MF9_CONF<5>	
1	1	0	MF9_CONF<6>	
1	1	1	MF9_CONF<7>	MSB

7.3.8. MF10 (3-bit LUT7/DFF10/LATCH10)

MF10 registers are listed in Table 7.32.

Table 7.32. MF10 (3-bit LUT7/DFF10/LATCH10) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF10 (3-bit LUT7/DFF10/LATCH10)				
0x5C00	<0>	MF10_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.29): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.30): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.29: Must be set to 1 in LATCH mode.
Note 7.30: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT7 uses 8-bit register to define its output function (see Table 7.33).

Table 7.33. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF10_CONF<0>	LSB
0	0	1	MF10_CONF<1>	
0	1	0	MF10_CONF<2>	
0	1	1	MF10_CONF<3>	
1	0	0	MF10_CONF<4>	
1	0	1	MF10_CONF<5>	
1	1	0	MF10_CONF<6>	
1	1	1	MF10_CONF<7>	MSB

7.3.9. MF11 (3-bit LUT8/DFF11/LATCH11)

MF11 registers are listed in Table 7.34.

Table 7.34. MF11 (3-bit LUT8/DFF11/LATCH11) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF11 (3-bit LUT8/DFF11/LATCH11)				
0x5D00	<0>	MF11_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.31): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.32): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.31: Must be set to 1 in LATCH mode.
Note 7.32: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT8 uses 8-bit register to define its output function (see Table 7.35).

Table 7.35. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF11_CONF<0>	LSB
0	0	1	MF11_CONF<1>	
0	1	0	MF11_CONF<2>	
0	1	1	MF11_CONF<3>	
1	0	0	MF11_CONF<4>	
1	0	1	MF11_CONF<5>	
1	1	0	MF11_CONF<6>	
1	1	1	MF11_CONF<7>	MSB

7.3.10. MF12 (3-bit LUT9/DFF12/LATCH12)

MF12 registers are listed in Table 7.36.

Table 7.36. MF12 (3-bit LUT9/DFF12/LATCH12) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF12 (3-bit LUT9/DFF12/LATCH12)				
0x5E00	<0>	MF12_CONF	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.33): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.34): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT control data: 0: LOW 1: HIGH

Note 7.33: Must be set to 1 in LATCH mode.

Note 7.34: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT9 uses 8-bit register to define its output function (see Table 7.37).

Table 7.37. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF12_CONF<0>	LSB
0	0	1	MF12_CONF<1>	
0	1	0	MF12_CONF<2>	
0	1	1	MF12_CONF<3>	
1	0	0	MF12_CONF<4>	
1	0	1	MF12_CONF<5>	
1	1	0	MF12_CONF<6>	
1	1	1	MF12_CONF<7>	MSB

7.4. MF (3-bit LUT/DFF/LATCH/8-bit PGEN) Macrocells

The AM1U1514 has a MF macrocell that can serve as either 3-bit LUT or as DFF/LATCH or as 8-bit PGEN.

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.38.

When the macrocells are used as DFF or LATCH, the three input signals from the connection matrix go to the data (D), clock/nlatch (CLK/nL) and (n)RST/(n)SET inputs of the DFF/LATCH, and the output goes back to the connection matrix. Operation of the DFF and LATCH are shown in the Table 7.39, Table 7.40.

When the macrocells are used as 8-bit PGEN function, the three input signals from the connection matrix go to the data (KEEP), clock (CLK) and ((n)RST) inputs of the 8-bit PGEN, and the output goes back to the connection matrix. The 8-bit PGEN macrocell outputs configurable pattern by the input clock (CLK) signal. The length of the pattern is configurable and can be selected from 2 to 8 bits. See Figure 7.5 and Figure 7.6.

Table 7.38. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

Table 7.39. Operation of the DFF

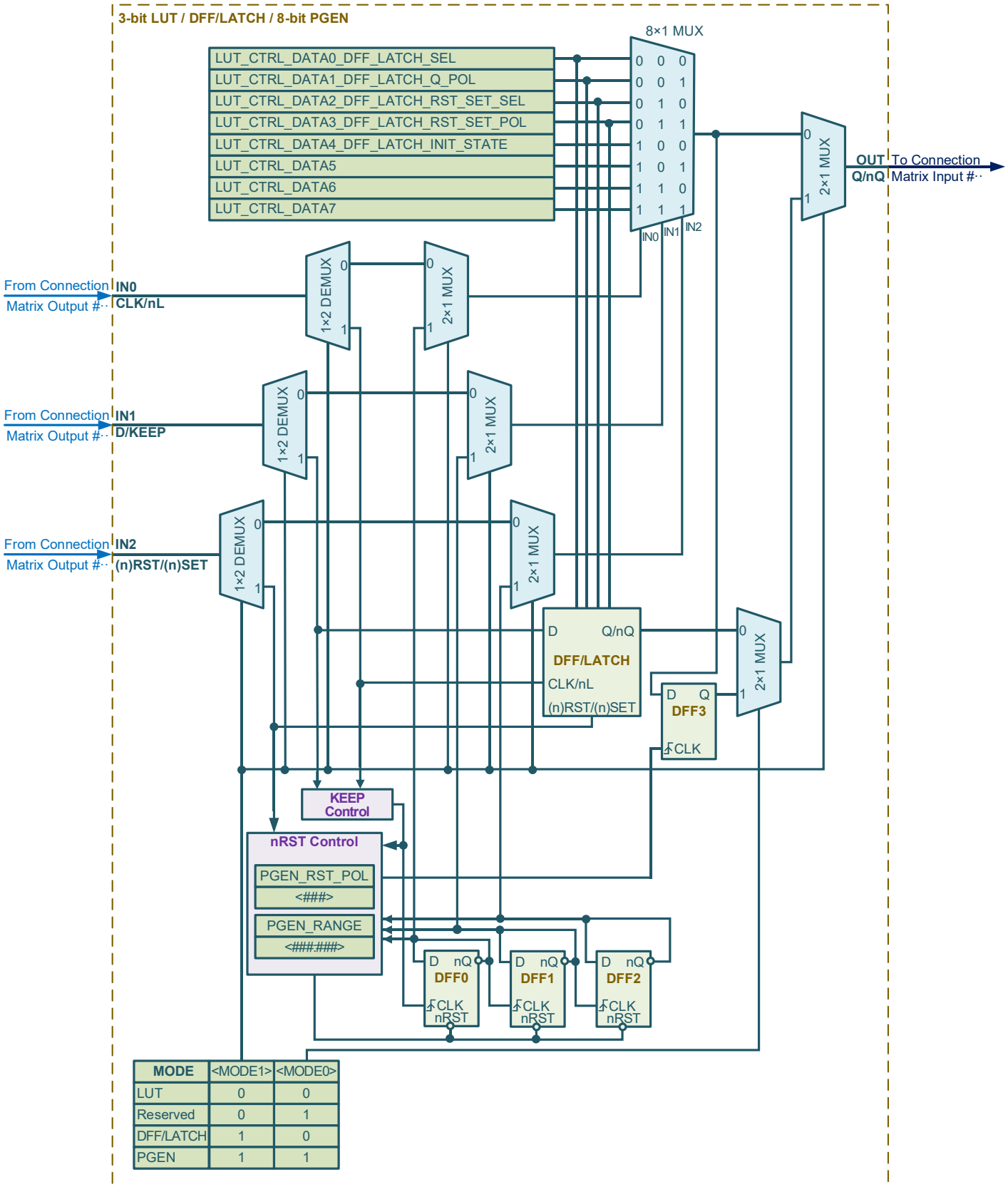
nRST/nSET	D	CLK	Q(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	⤓	0/1
1	0	⤒	t–1
1	1	⤓	1/0
1	1	⤒	t–1

Note 7.35: X – Don't Care
Note 7.36: t–1 – Previous State

Table 7.40. Operation of the LATCH

nSET	nL	D	Q(t)/nQ(t)
nSET = 0	X	X	1/0
1	0	0	t–1
1	0	1	t–1
1	1	0	0/1
1	1	1	1/0

Note 7.37: X – Don't Care
Note 7.38: t–1 – Previous State



MF#	IN0/CLK/nL	IN1/D/KEEP	IN2/(n)RST/(n)SET	OUT/Q/nQ
MF13 (3-bit LUT10/DFF13/LATCH13)	CMO38	CMO39	CMO40	CMI16
MF14 (3-bit LUT11/DFF14/LATCH14)	CMO41	CMO42	CMO43	CMI17

Figure 7.5. Schematic diagram of MF (3-bit LUT/DFF/LATCH/8-bit PGEN)

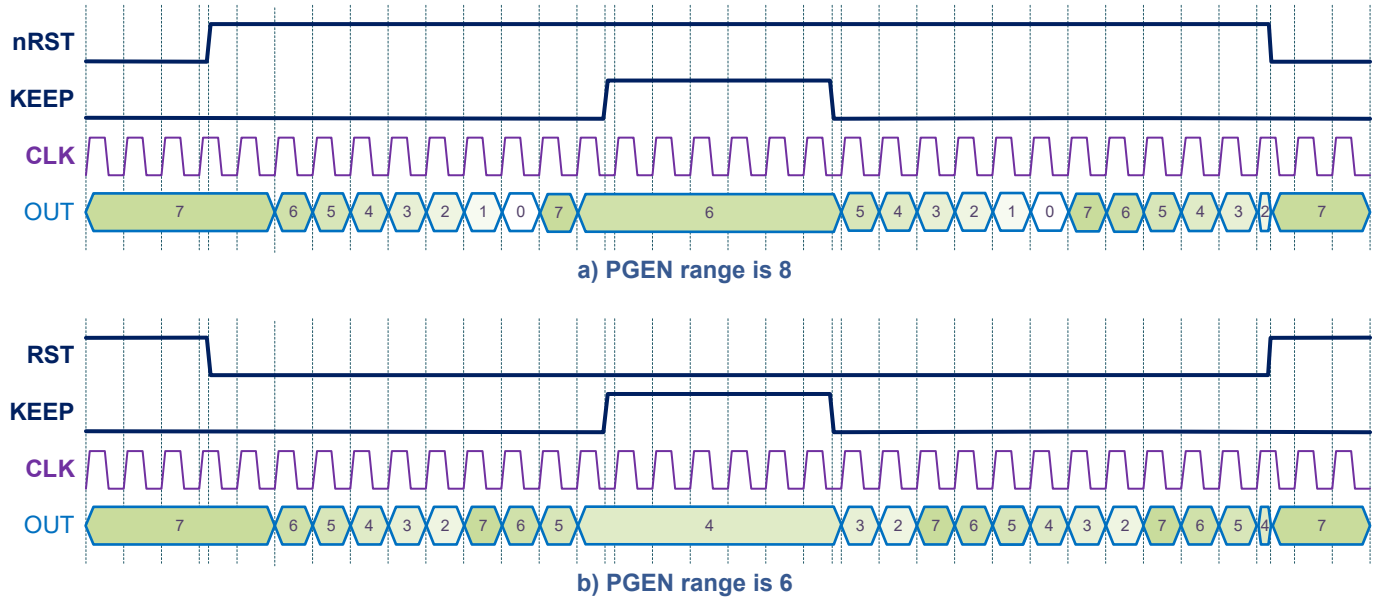


Figure 7.6. Timing diagrams of 8-bit PGEN

7.4.1. MF13 (3-bit LUT10/DFF13/LATCH13/8-bit PGEN0)

MF13 registers are listed in Table 7.41.

Table 7.41. MF13 (3-bit LUT10/DFF13/LATCH13/8-bit PGEN0) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF13 (3-bit LUT10/DFF13/LATCH13/8-bit PGEN0)				
0x5F00	<1:0>	MF13_CONF0	MODE	MF mode: 00: LUT 01: Reserved 10: DFF/LATCH 11: PGEN
	<2>		PGEN_RST_POL	Reset polarity: 0: nRST 1: RST
	<3>			Reserved
	<6:4>		PGEN_RANGE	PGEN range: 000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8
	<7>			Reserved
0x5F01	<0>	MF13_CONF1	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT or PGEN control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT or PGEN control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT or PGEN control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.39): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT or PGEN control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT or PGEN control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.40): 0: LOW 1: HIGH
	<5>		LUT_CTRL_DATA5	5th bit of LUT or PGEN control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT or PGEN control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT or PGEN control data: 0: LOW 1: HIGH

Note 7.39: Must be set to 1 in LATCH mode.
Note 7.40: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT10 uses 8-bit register to define its output function (Table 7.42).

Table 7.42. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF13_CONF1<0>	LSB
0	0	1	MF13_CONF1<1>	
0	1	0	MF13_CONF1<2>	
0	1	1	MF13_CONF1<3>	
1	0	0	MF13_CONF1<4>	
1	0	1	MF13_CONF1<5>	
1	1	0	MF13_CONF1<6>	
1	1	1	MF13_CONF1<7>	MSB

7.4.2. MF14 (3-bit LUT11/DFF14/LATCH14/8-bit PGEN1)

MF14 registers are listed in Table 7.43.

Table 7.43. MF14 (3-bit LUT11/DFF14/LATCH14/8-bit PGEN1) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF14 (3-bit LUT11/DFF14/LATCH14/8-bit PGEN1)				
0x6000	<1:0>	MF14_CONF0	MODE	MF mode: 00: LUT 01: Reserved 10: DFF/LATCH 11: PGEN
	<2>		PGEN_RST_POL	Reset polarity: 0: nRST 1: RST
	<3>			Reserved
	<6:4>		PGEN_RANGE	PGEN range: 000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8
	<7>			Reserved
0x6001	<0>	MF14_CONF1	LUT_CTRL_DATA0_DFF_LATCH_SEL	0th bit of LUT or PGEN control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
	<1>		LUT_CTRL_DATA1_DFF_LATCH_Q_POL	1st bit of LUT or PGEN control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
	<2>		LUT_CTRL_DATA2_DFF_LATCH_RST_SET_SEL	2nd bit of LUT or PGEN control data: 0: LOW 1: HIGH or DFF reset/set selection (Note 7.41): 0: (n)RST 1: (n)SET
	<3>		LUT_CTRL_DATA3_DFF_LATCH_RST_SET_POL	3rd bit of LUT or PGEN control data: 0: LOW 1: HIGH or reset/set polarity: 0: nRST(nSET) 1: RST(SET)
	<4>		LUT_CTRL_DATA4_DFF_INIT_STATE	4th bit of LUT or PGEN control data: 0: LOW 1: HIGH or Initial state of DFF (Note 7.42): 0: LOW 1: HIGH

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<5>		LUT_CTRL_DATA5	5th bit of LUT or PGEN control data: 0: LOW 1: HIGH
	<6>		LUT_CTRL_DATA6	6th bit of LUT or PGEN control data: 0: LOW 1: HIGH
	<7>		LUT_CTRL_DATA7	7th bit of LUT or PGEN control data: 0: LOW 1: HIGH

Note 7.41: Must be set to 1 in LATCH mode.

Note 7.42: In Latch mode, initial state is always High; this bit is applicable in DFF mode.

The 3-bit LUT11 uses 8-bit register to define its output function (Table 7.44).

Table 7.44. 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF14_CONF1<0>	LSB
0	0	1	MF14_CONF1<1>	
0	1	0	MF14_CONF1<2>	
0	1	1	MF14_CONF1<3>	
1	0	0	MF14_CONF1<4>	
1	0	1	MF14_CONF1<5>	
1	1	0	MF14_CONF1<6>	
1	1	1	MF14_CONF1<7>	MSB

7.5. MF (3-bit LUT/Shift Register) Macrocell

The MF macrocell has a capability to serve as either a 3-bit LUT or as a Shift Register (SHR).

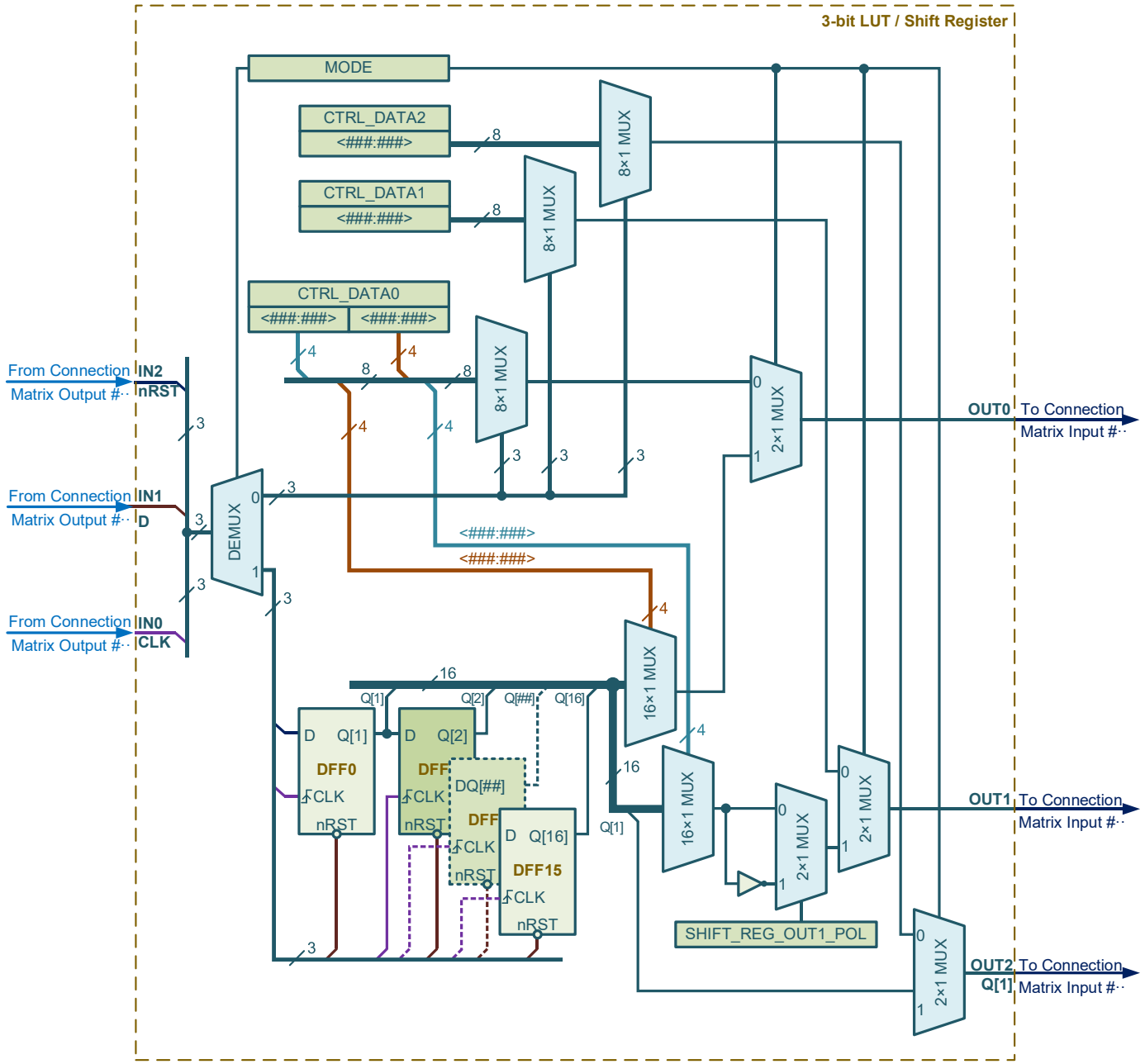
When the MF macrocell is used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces three outputs, that go back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.45.

The Shift Register contains sixteen stages cascade of positive edge triggered DFFs. The signal from any stage can be routed to OUT0 and OUT1 independently. The Q[1] output is always connected to the output of the first stage. The Shift Register has Data (D), Clock (CLK) and Reset (nRST) inputs from connection matrix. Applying low-level signal to the nRST sets all stage values to zero.

Schematic diagram of 3-bit LUT12/Shift Register macrocell is shown on Figure 7.7.

Table 7.45. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1



MF#	IN0/CLK	IN1/D	IN2/nRST	OUT0	OUT1	OUT2
MF15 (3-bit LUT12/Shift Register)	CMO44	CMO45	CMO46	CMI18	CMI19	CMI20

Figure 7.7. Schematic diagram of MF15 (3-bit LUT12/Shift Register)

7.5.1. MF15 (3-bit LUT12/Shift Register) Macrocell

MF15 registers are listed in Table 7.46.

Table 7.46. MF15 (3-bit LUT12/Shift Register) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF15 (3-bit LUT12/Shift Register)				
0x6100	<0>	MF15_CONF	MODE	MF mode: 0: LUT 1: Shift register
	<1>		SHIFT_REG_OUT1_POL	Shift register OUT1 polarity: 0: OUT1 1: nOUT1
	<3:2>			Reserved
	<4>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<5>			Reserved
	<6>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7>			Reserved
0x6101	<0>	MF15_CTRL_DATA0	LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0	Low tetrad of OUT0 LUT control data or stage of OUT0 shift register
	<7>		LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1	High tetrad of OUT0 LUT control data or stage of OUT1 shift register
0x6102	<7:0>	MF15_CTRL_DATA1		OUT1 LUT control data
0x6103	<7:0>	MF15_CTRL_DATA2		OUT2 LUT control data

The 3-bit LUT12 uses three 8-bit registers to define its outputs function (see Table 7.47).

Table 7.47. 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT0	OUT1	OUT2	
0	0	0	MF15_CTRL_DATA0<0>	MF15_CTRL_DATA1<0>	MF15_CTRL_DATA2<0>	LSB
0	0	1	MF15_CTRL_DATA0<1>	MF15_CTRL_DATA1<1>	MF15_CTRL_DATA2<1>	
0	1	0	MF15_CTRL_DATA0<2>	MF15_CTRL_DATA1<2>	MF15_CTRL_DATA2<2>	
0	1	1	MF15_CTRL_DATA0<3>	MF15_CTRL_DATA1<3>	MF15_CTRL_DATA2<3>	
1	0	0	MF15_CTRL_DATA0<4>	MF15_CTRL_DATA1<4>	MF15_CTRL_DATA2<4>	
1	0	1	MF15_CTRL_DATA0<5>	MF15_CTRL_DATA1<5>	MF15_CTRL_DATA2<5>	
1	1	0	MF15_CTRL_DATA0<6>	MF15_CTRL_DATA1<6>	MF15_CTRL_DATA2<6>	
1	1	1	MF15_CTRL_DATA0<7>	MF15_CTRL_DATA1<7>	MF15_CTRL_DATA2<7>	MSB

7.6. MF (3-bit LUT/8-bit TMR) Macrocells

Six macrocells have the capability to serve as either 3-bit LUTs or as 8-bit timer (TMR).

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.48.

When the macrocells are used as 8-bit TMR function, the three input signals from the connection matrix go to the EXTCLK, IN(RST for Counter mode) and KEEP inputs of the 8-bit TMR, and the output goes back to the connection matrix.

Each timer has the following mode of operation:

- Delay
- Counter
- One Shot
- Frequency Detector
- Delayed Edge Detector
- Edge Detector

The output polarity of the TMR is configurable and can be selected as non-inverted or inverted.

The KEEP input allows to pause counting by applying HIGH level to KEEP, the counting is resume after KEEP goes LOW.

In the Delay mode the TMR delays the input signal by the selected edge event (rising edge, falling edge, both edges) for a time determined by the Control Data, input clock signal and selected divider value. If input signal is shorter than the delay value, the signal does not propagate to the output. The timing diagrams of this mode is shown in the Figure 7.9.

In the Counter mode the TMR divides input clock signal by the value determined by the Control Data, input clock signal and selected divider value. The output of the TMR goes HIGH every time when the Counted Value (current value of the counter) is equal 0. The RST in of the TMR reset Counted value to 0 by one of the following events: rising edge, falling edge, both edges, high level. The timing diagrams of this mode is shown in the Figure 7.10.

In One-Shot mode this macrocell generates a high-level pulse with a set width, when detecting the edge event, which is selectable by the registers, on its IN input. The pulse width is determined by the Control Data, input clock signal and selected divider value. Any incoming edges are ignored during pulse width generation. The timing diagrams of this mode is shown in the Figure 7.11.

In Frequency Detector mode the TMR function following scenarios:

- Rising Edge: The output will go HIGH if the time between two rising edges is less than the delay.
  The output will go LOW if the next rising edge has not come after the last rising edge in specified time.
- Falling Edge: The output will go HIGH if the time between two falling edges is less than the set time.
  The output will go LOW if the next falling edge has not come after the last falling edge in specified time.
- Both Edges: The output will go HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse.
  The output will go LOW if the next rising/falling edge has not come after the last falling/rising edge in specified time.

The timing diagrams of the Frequency Detector Mode is shown in the Figure 7.12.

In the Delayed Edge Detector mode the TMR generates delayed short high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The delay time is determined by the Control Data, input clock signal and selected divider value. The timing diagrams of this mode is shown in the Figure 7.13.

In Edge Detector mode the TMR generates short high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The timing diagrams of this mode is shown in the Figure 7.14.

Time of Timers for each mode can be calculated using the following formulas (Note 7.43, Note 7.44):

- Delay (Figure 7.9)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK};
- Counter (Figure 7.10)
  Output Period = (Control Data + 1)/F_{CLK};
  Output Frequency = F_{CLK}/(Control Data + 1);
- One Shot (Figure 7.11)
  Pulse width = (Control Data + 1 + VAR)/F_{CLK};
- Frequency Detector (Figure 7.12)
  Detected Frequency = F_{CLK}/(Control Data + 1 + VAR);
- Delayed Edge Detector (Figure 7.13)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK}.

Note 7.43 F_{CLK} – CLK input frequency.

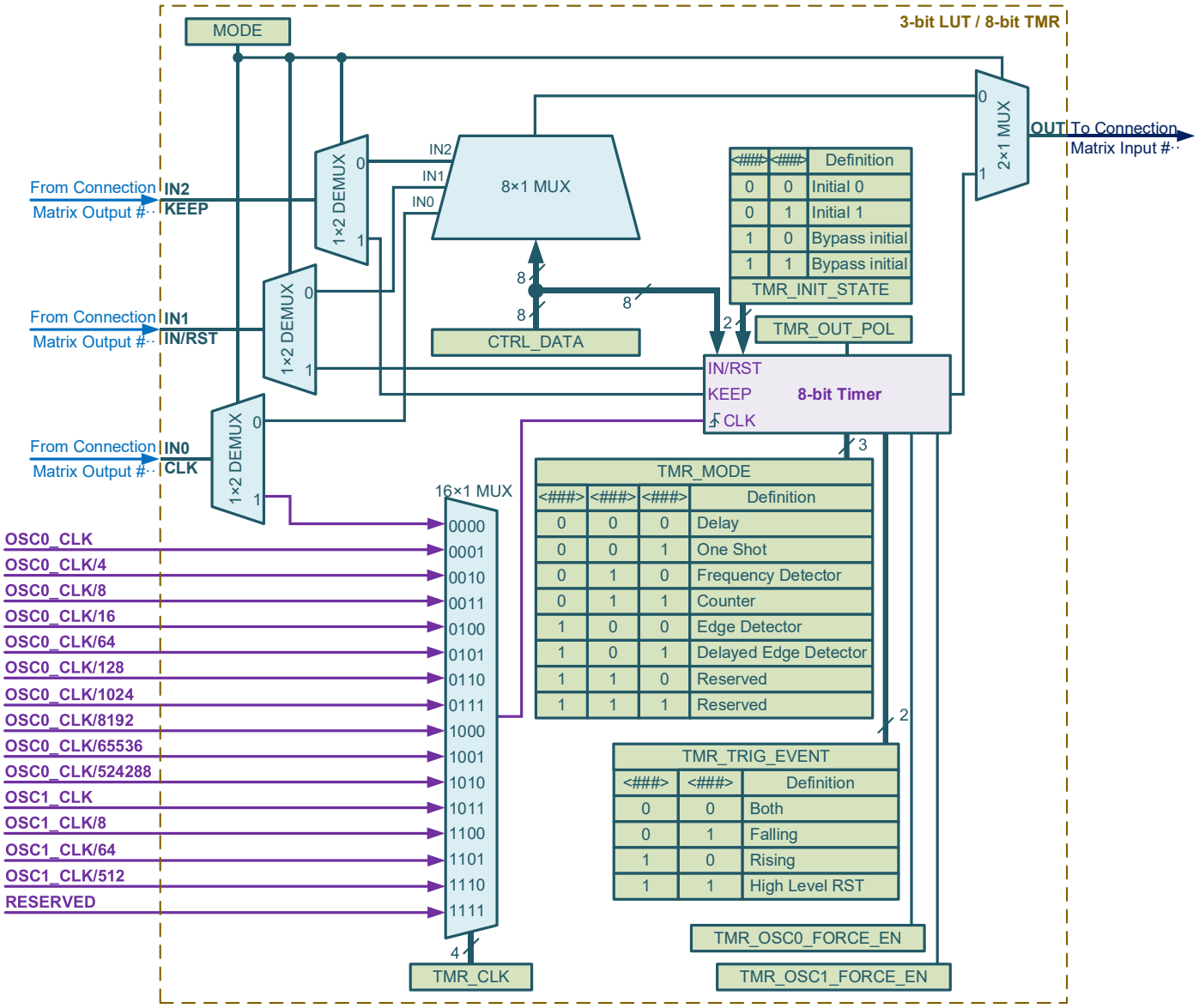
Note 7.44 VAR = 0…1 – defined by the asynchronous time between the input signal and the first clock pulse.

Note 7.45 Counters initialize with Control Data after POR.

Each TMR has two configuration bits that enable to force OSC0 and OSC1 by the TMR when it is required to perform its function.

Table 7.48. 3-bit LUT Truth Table of Standard Logic Gates

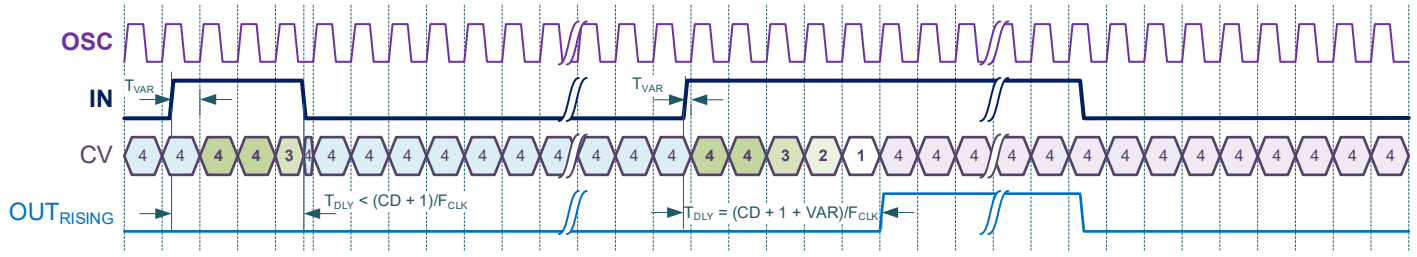
Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1



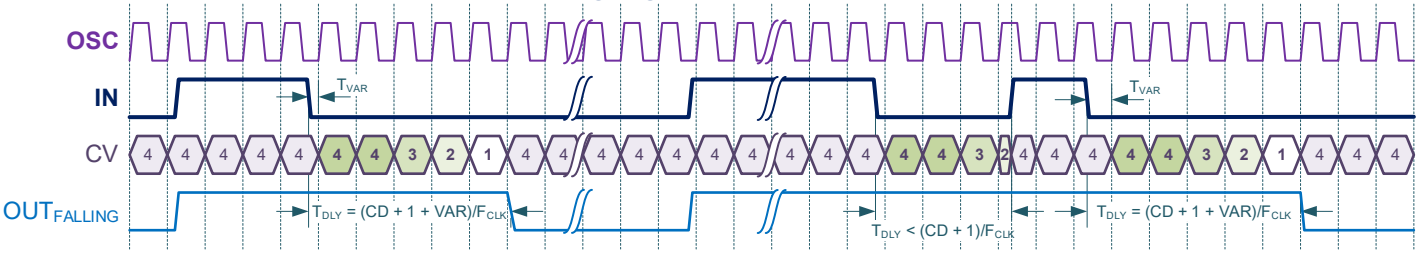
MF#	IN0/CLK	IN1/IN/RST	IN2/KEEP	OUT
MF16 (3-bit LUT13/8-bit TMR0)	CMO47	CMO48	CMO49	CMI21
MF17 (3-bit LUT14/8-bit TMR1)	CMO50	CMO51	CMO52	CMI22
MF18 (3-bit LUT15/8-bit TMR2)	CMO53	CMO54	CMO55	CMI23
MF19 (3-bit LUT16/8-bit TMR3)	CMO56	CMO57	CMO58	CMI24
MF20 (3-bit LUT17/8-bit TMR4)	CMO59	CMO60	CMO61	CMI25
MF21 (3-bit LUT18/8-bit TMR5)	CMO62	CMO63	CMO64	CMI26

Figure 7.8. MF (3-bit LUT/8-bit TMR)

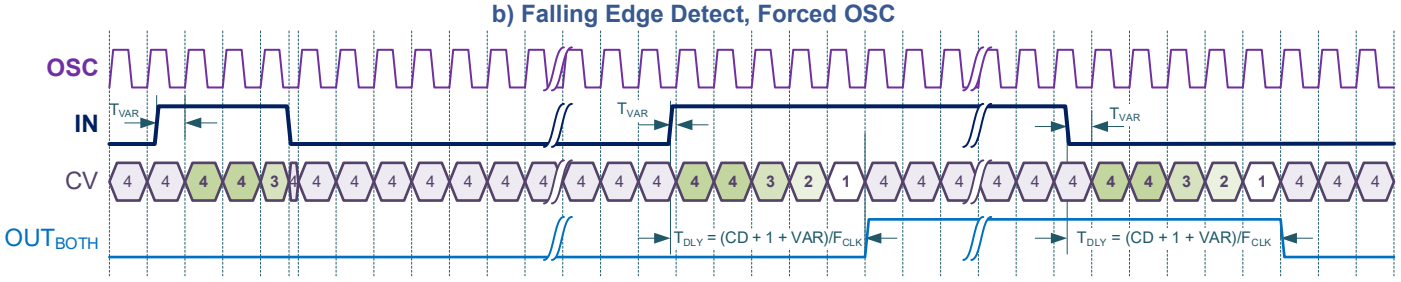
7.6.1. TMR Timing Diagrams



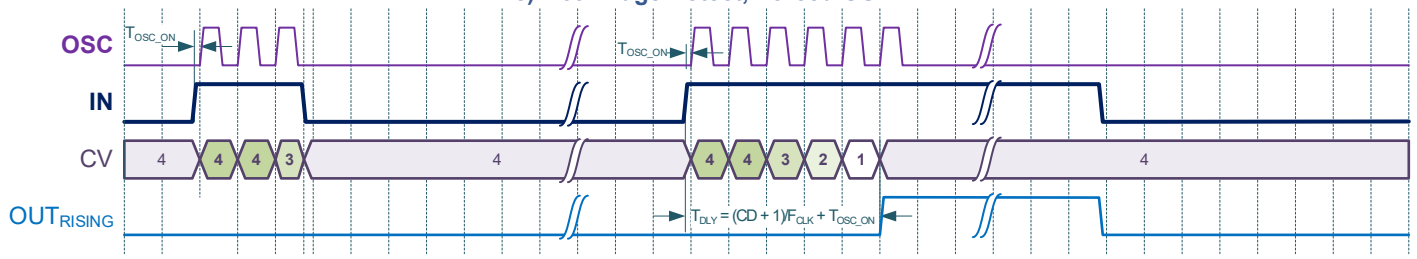
a) Rising Edge Detect, Forced OSC



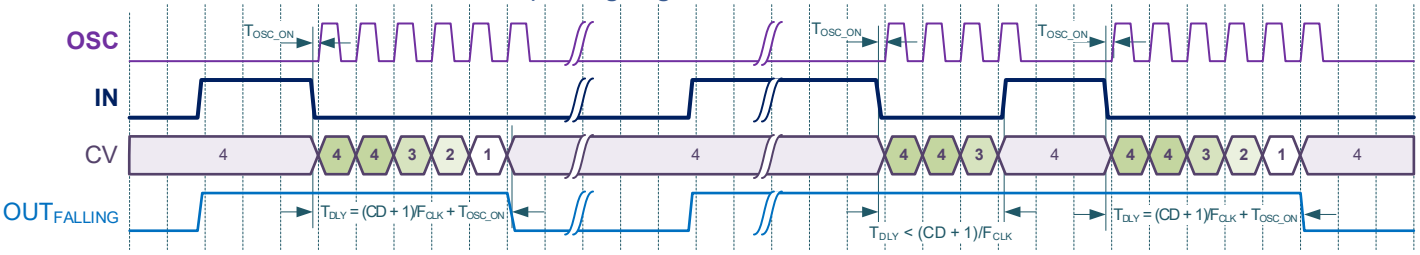
b) Falling Edge Detect, Forced OSC



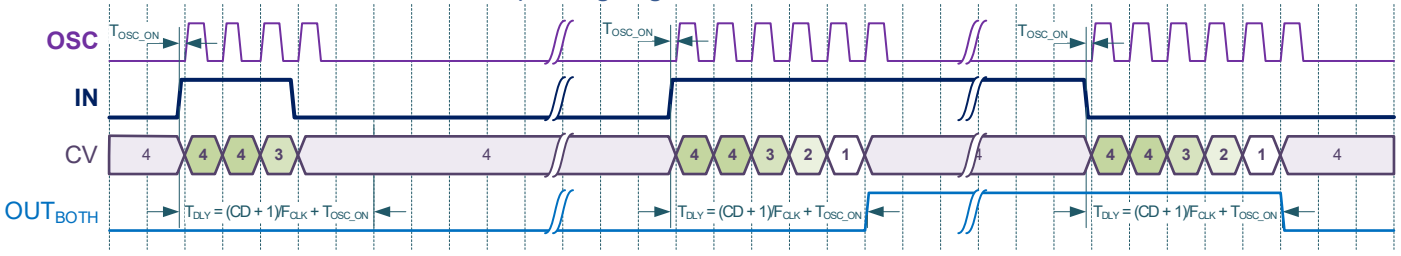
c) Both Edge Detect, Forced OSC



d) Rising Edge Detect, Auto OSC

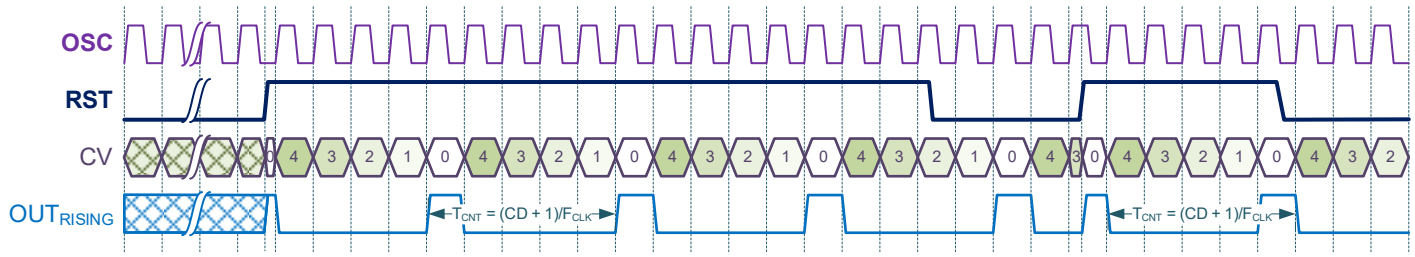


e) Falling Edge Detect, Auto OSC

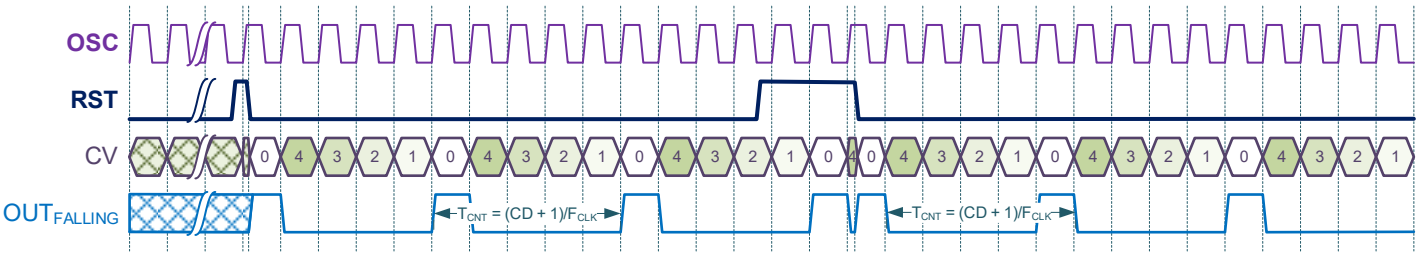


f) Both Edge Detect, Auto OSC

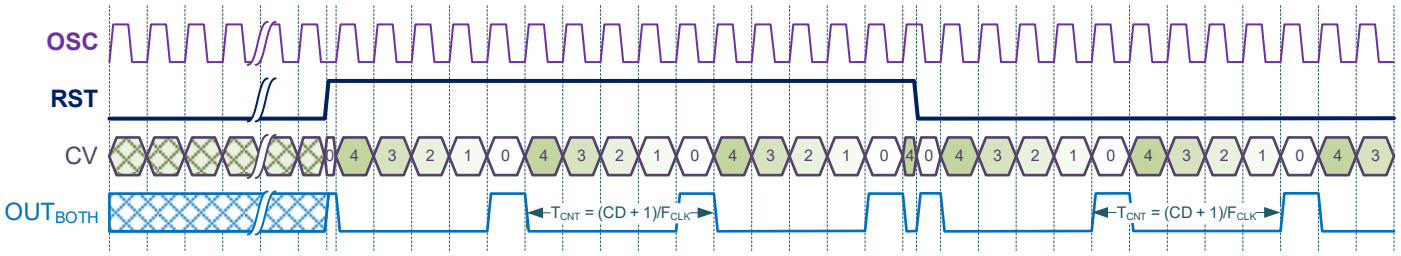
Figure 7.9. Delay Mode (Control Data: 4)



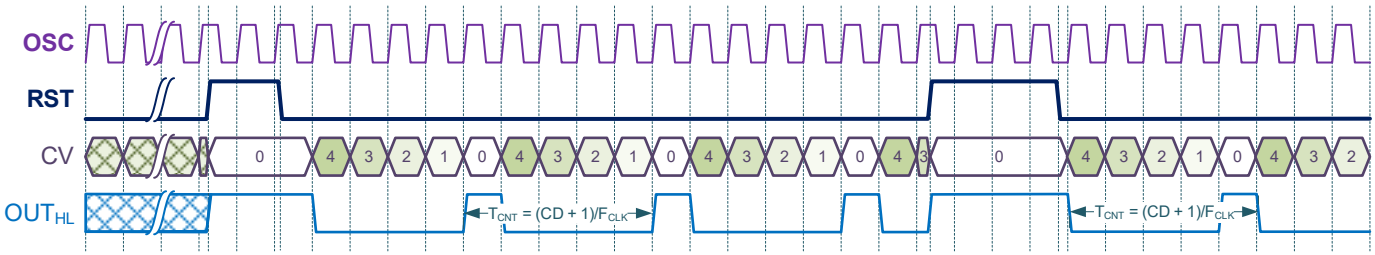
a) Rising Reset



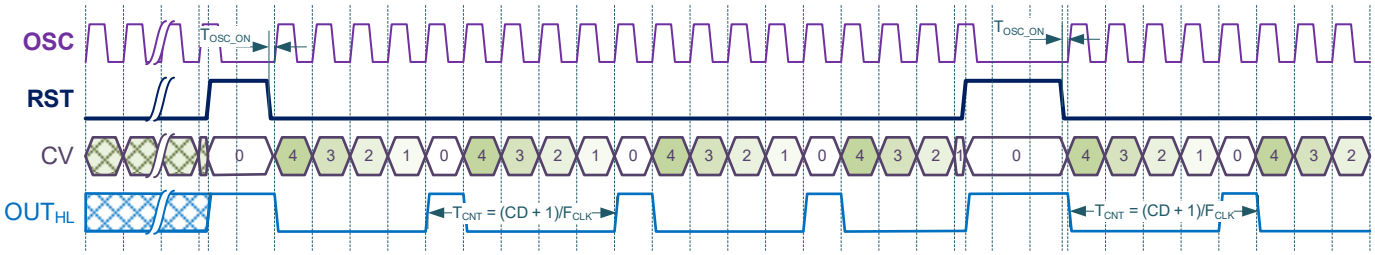
b) Falling Reset



c) Both Edge Reset

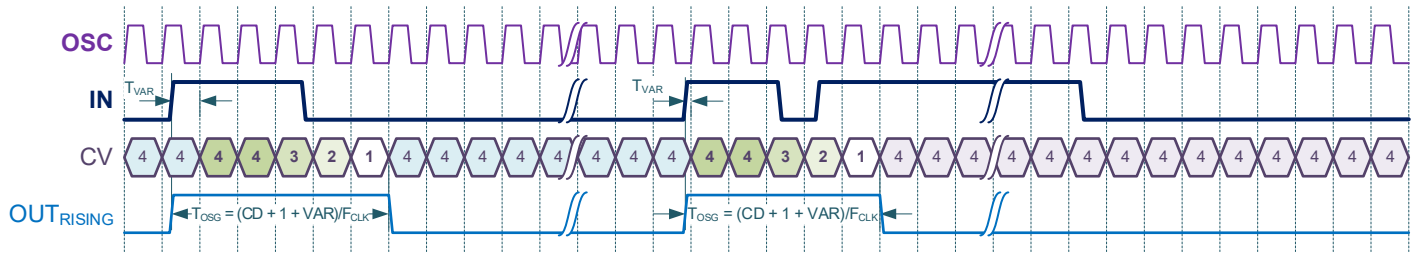


d) High Level Reset, Forced OSC

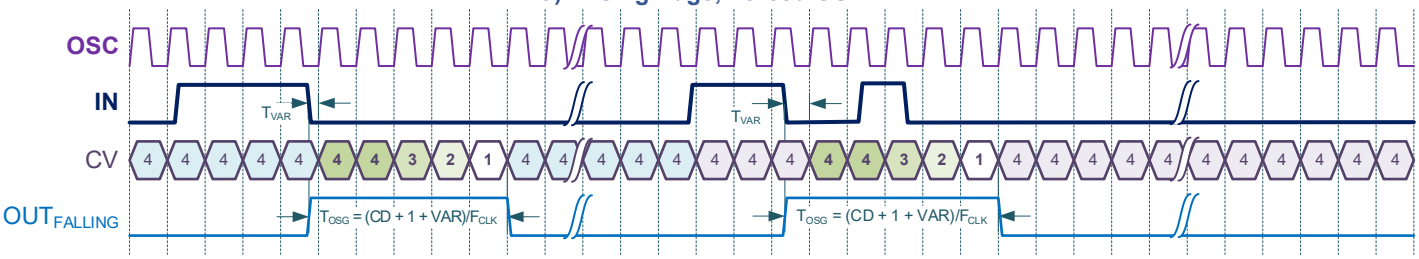


e) High Level Reset, Auto OSC

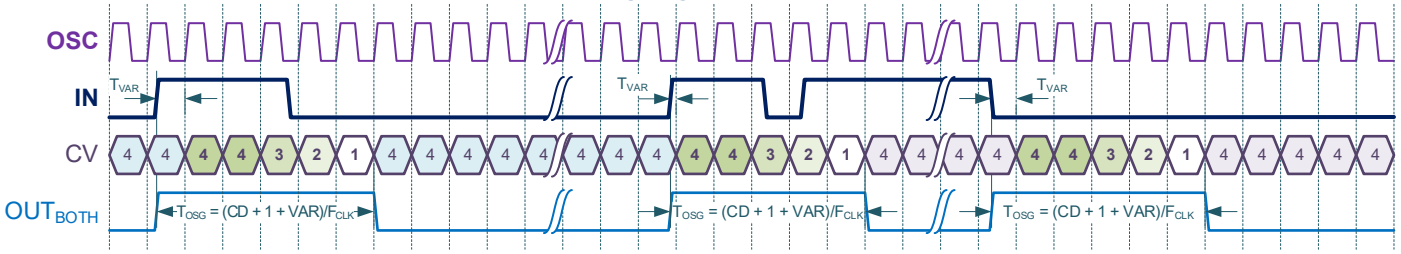
Figure 7.10. Counter Mode (Control Data: 4)



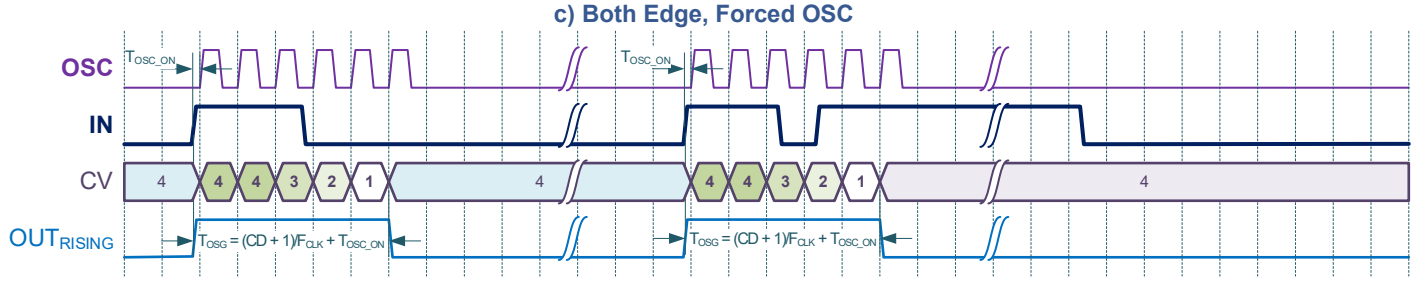
a) Rising Edge, Forced OSC



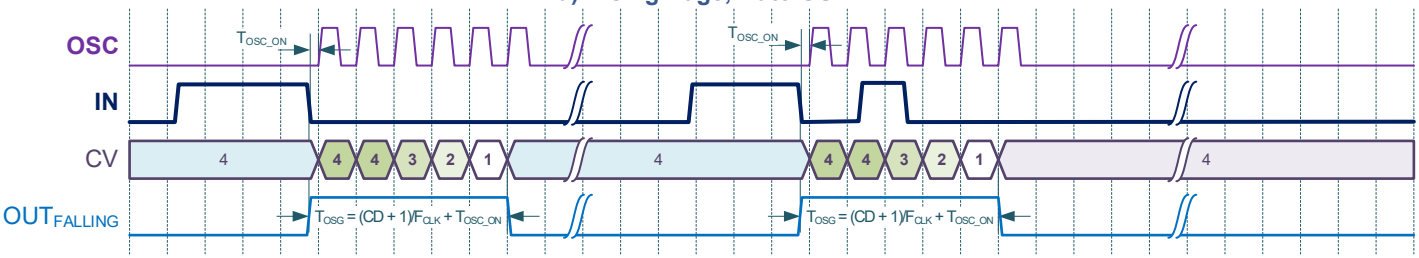
b) Falling Edge, Forced OSC



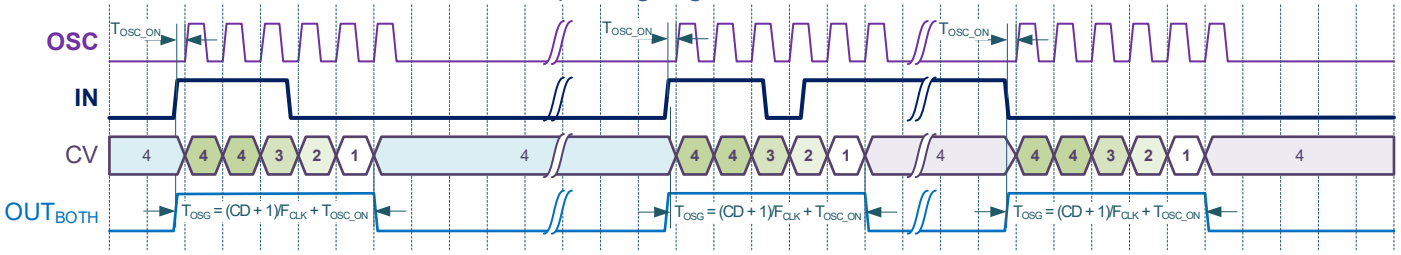
c) Both Edge, Forced OSC



d) Rising Edge, Auto OSC

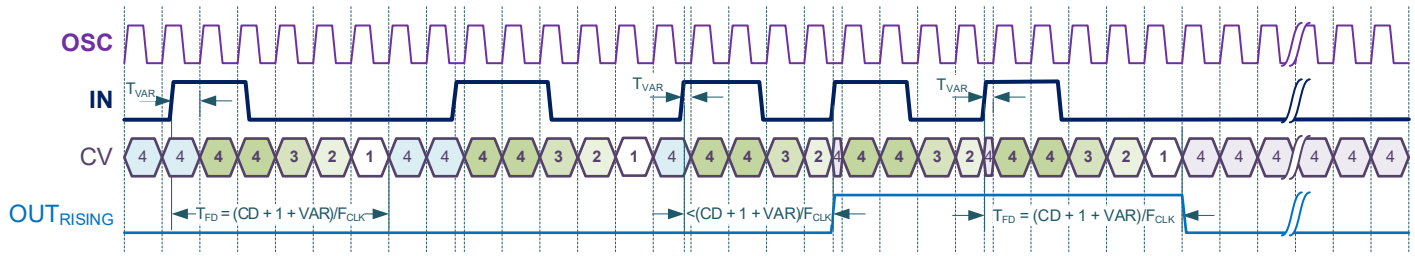


e) Falling Edge, Auto OSC

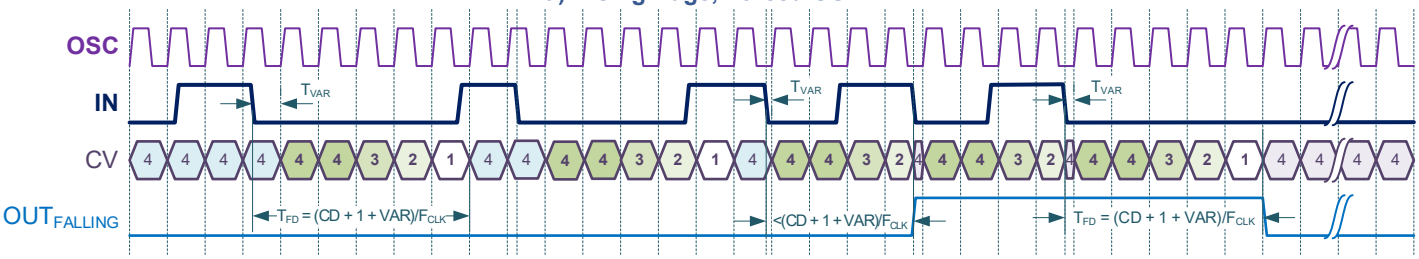


f) Both Edge, Auto OSC

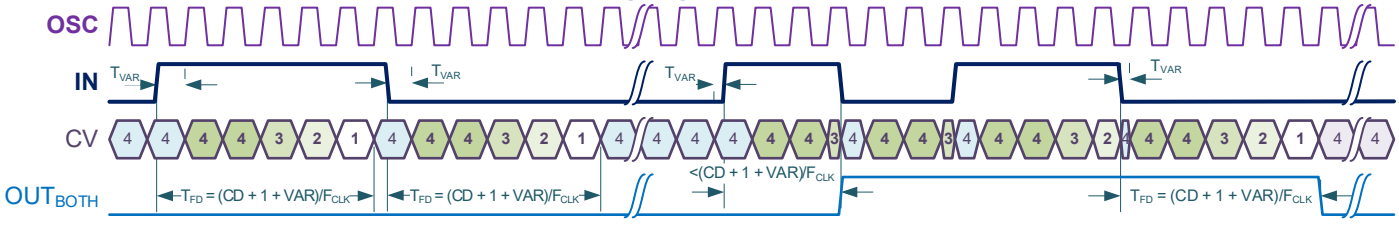
Figure 7.11. One-Shot Generator Mode (Control Data: 4)



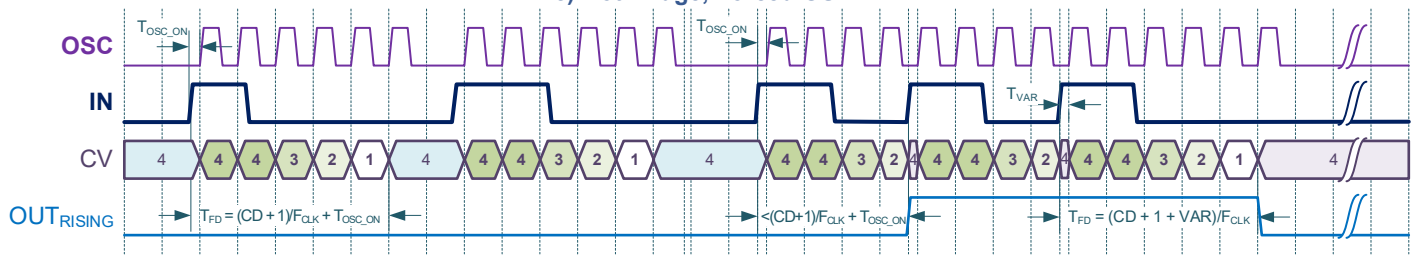
a) Rising Edge, Forced OSC



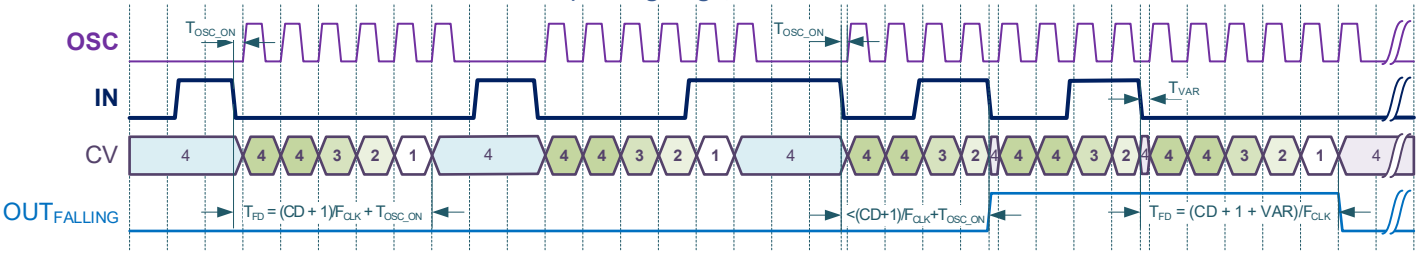
b) Falling Edge, Forced OSC



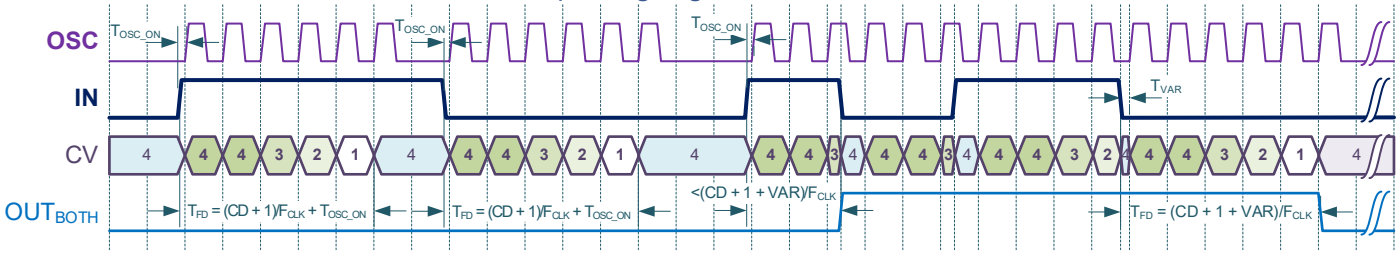
c) Both Edge, Forced OSC



d) Rising Edge, Auto OSC



e) Falling Edge, Auto OSC



f) Both Edge, Auto OSC

Figure 7.12. Frequency Detector Mode (Control Data: 4)

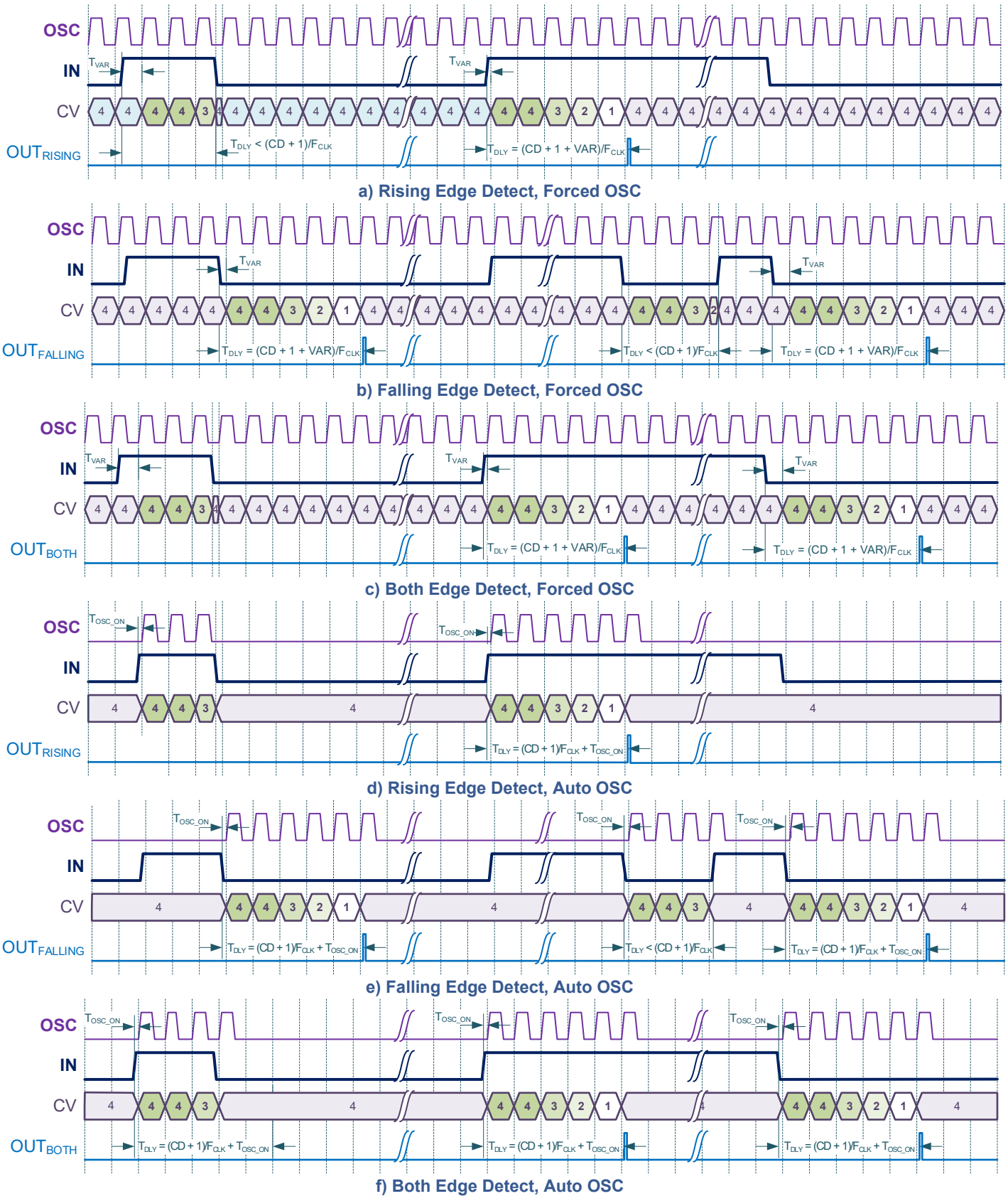


Figure 7.13. Delay Edge Detector Mode (Control Data: 4)

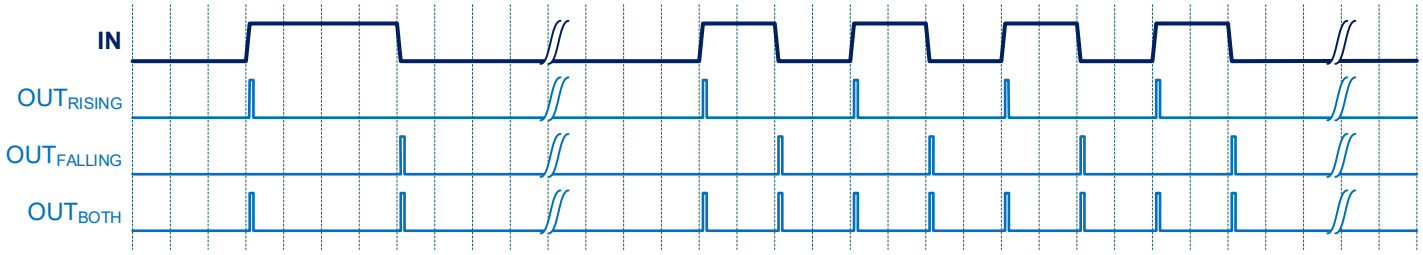


Figure 7.14. Edge Detector Mode

7.6.2. MF16 (3-bit LUT13/8-bit TMR0)

MF16 registers are listed in Table 7.49.

Table 7.49. MF16 (3-bit LUT13/8-bit TMR0) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF16 (3-bit LUT13/8-bit TMR0)				
0x6200	<0>	MF16_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
0x6201	<3:0>	MF16_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.46) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>			Reserved
0x6202	<7:0>	MF16_CTRL_DATA		MF control data

Note 7.46 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 3-bit LUT13 uses 8-bit register to define its output function (see Table 7.50).

Table 7.50. 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF16_CTRL_DATA<0>	LSB
0	0	1	MF16_CTRL_DATA<1>	
0	1	0	MF16_CTRL_DATA<2>	
0	1	1	MF16_CTRL_DATA<3>	
1	0	0	MF16_CTRL_DATA<4>	
1	0	1	MF16_CTRL_DATA<5>	
1	1	0	MF16_CTRL_DATA<6>	
1	1	1	MF16_CTRL_DATA<7>	MSB

7.6.3. MF17 (3-bit LUT14/8-bit TMR1)

MF17 registers are listed in Table 7.51.

Table 7.51. MF17 (3-bit LUT14/8-bit TMR1) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF17 (3-bit LUT14/8-bit TMR1)				
0x6300	<0>	MF17_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
0x6301	<3:0>	MF17_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.47) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>			Reserved
0x6302	<7:0>	MF17_CTRL_DATA		MF control data

Note 7.47 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 3-bit LUT14 uses 8-bit register to define its output function (see Table 7.52).

Table 7.52. 3-bit LUT14 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF17_CTRL_DATA<0>	LSB
0	0	1	MF17_CTRL_DATA<1>	
0	1	0	MF17_CTRL_DATA<2>	
0	1	1	MF17_CTRL_DATA<3>	
1	0	0	MF17_CTRL_DATA<4>	
1	0	1	MF17_CTRL_DATA<5>	
1	1	0	MF17_CTRL_DATA<6>	
1	1	1	MF17_CTRL_DATA<7>	MSB

7.6.4. MF18 (3-bit LUT15/8-bit TMR2)

MF18 registers are listed in Table 7.53.

Table 7.53. MF18 (3-bit LUT15/8-bit TMR2) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF18 (3-bit LUT15/8-bit TMR2)				
0x6400	<0>	MF18_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
0x6401	<3:0>	MF18_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.48) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>			Reserved
0x6402	<7:0>	MF18_CTRL_DATA		MF control data

Note 7.48 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 3-bit LUT15 uses 8-bit register to define its output function (see Table 7.54).

Table 7.54. 3-bit LUT15 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF18_CTRL_DATA<0>	LSB
0	0	1	MF18_CTRL_DATA<1>	
0	1	0	MF18_CTRL_DATA<2>	
0	1	1	MF18_CTRL_DATA<3>	
1	0	0	MF18_CTRL_DATA<4>	
1	0	1	MF18_CTRL_DATA<5>	
1	1	0	MF18_CTRL_DATA<6>	
1	1	1	MF18_CTRL_DATA<7>	MSB

7.6.5. MF19 (3-bit LUT16/8-bit TMR3)

MF19 registers are listed in Table 7.55.

Table 7.55. MF19 (3-bit LUT16/8-bit TMR3) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF19 (3-bit LUT16/8-bit TMR3)				
0x6500	<0>	MF19_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
0x6501	<3:0>	MF19_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.49) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
0x6502	<7:0>	MF19_CTRL_DATA		MF control data

Note 7.49 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 3-bit LUT16 uses 8-bit register to define its output function (see Table 7.56).

Table 7.56. 3-bit LUT16 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF19_CTRL_DATA<0>	LSB
0	0	1	MF19_CTRL_DATA<1>	
0	1	0	MF19_CTRL_DATA<2>	
0	1	1	MF19_CTRL_DATA<3>	
1	0	0	MF19_CTRL_DATA<4>	
1	0	1	MF19_CTRL_DATA<5>	
1	1	0	MF19_CTRL_DATA<6>	
1	1	1	MF19_CTRL_DATA<7>	MSB

7.6.6. MF20 (3-bit LUT17/8-bit TMR4)

MF20 registers are listed in Table 7.57.

Table 7.57. MF20 (3-bit LUT17/8-bit TMR4) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF20 (3-bit LUT17/8-bit TMR4)				
0x6600	<0>	MF20_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
0x6601	<3:0>	MF20_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.50) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>			Reserved
0x6602	<7:0>	MF20_CTRL_DATA		MF control data

Note 7.50 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 3-bit LUT17 uses 8-bit register to define its output function (see Table 7.58).

Table 7.58. 3-bit LUT17 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF20_CTRL_DATA<0>	LSB
0	0	1	MF20_CTRL_DATA<1>	
0	1	0	MF20_CTRL_DATA<2>	
0	1	1	MF20_CTRL_DATA<3>	
1	0	0	MF20_CTRL_DATA<4>	
1	0	1	MF20_CTRL_DATA<5>	
1	1	0	MF20_CTRL_DATA<6>	
1	1	1	MF20_CTRL_DATA<7>	MSB

7.6.7. MF21 (3-bit LUT18/8-bit TMR5)

MF21 registers are listed in Table 7.59.

Table 7.59. MF21 (3-bit LUT18/8-bit TMR5) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF21 (3-bit LUT18/8-bit TMR5)				
0x6700	<0>	MF21_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
0x6701	<3:0>	MF21_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.51) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
0x6702	<7:0>	MF21_CTRL_DATA		MF control data

Note 7.51 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 3-bit LUT18 uses 8-bit register to define its output function (see Table 7.60).

Table 7.60. 3-bit LUT18 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF21_CTRL_DATA<0>	LSB
0	0	1	MF21_CTRL_DATA<1>	
0	1	0	MF21_CTRL_DATA<2>	
0	1	1	MF21_CTRL_DATA<3>	
1	0	0	MF21_CTRL_DATA<4>	
1	0	1	MF21_CTRL_DATA<5>	
1	1	0	MF21_CTRL_DATA<6>	
1	1	1	MF21_CTRL_DATA<7>	MSB

7.7. MF (4-bit LUT/16-bit TMR) Macrocells

Two macrocells have the capability to serve as 4-bit LUT or as 16-bit Timer (TMR).

When the MF macrocells are configured as LUT, the 4-bit LUT receives four input signals from the connection matrix and generates a single output, which is routed back into the connection matrix. The LUT allows the implementation of user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.61.

When the macrocells are configured as 16-bit timer, four input signals from the connection matrix go to the external clock (EXTCLK), IN (RST for Counter mode), KEEP and UP. The output signal is routed back to the connection matrix.

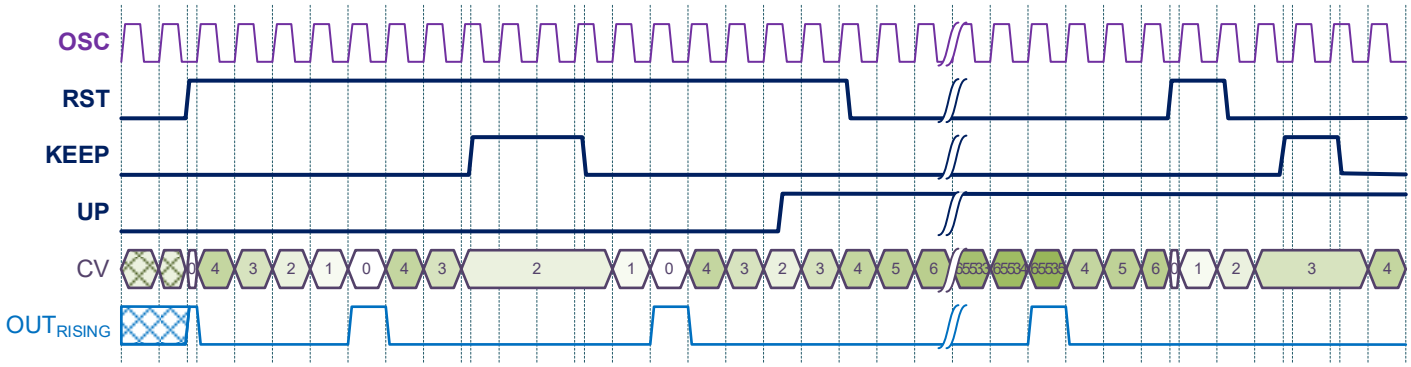
The counting direction is controlled by the UP input. When the UP input is LOW, the counter decrements; when HIGH, the counter increments (Note 7.52). Counting can be paused by applying a HIGH level to the KEEP input. The count resumes when the level goes LOW. Timing diagrams are shown in Figure 7.15.

Note 7.52: The UP input is sampled on each clock edge. After power-up, the counting direction is established by the first clock edge.

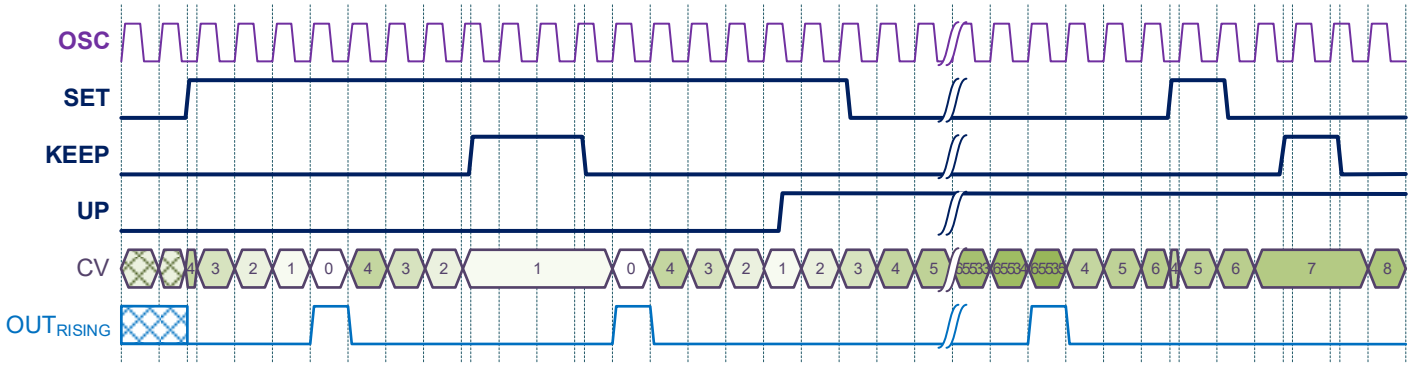
Descriptions of Delay Mode, Counter Mode, One-Shot Mode, Frequency Mode, Edge Detect Mode and Delayed Edge Detect Mode are provided section 7.5 and corresponding timing diagrams in section 7.6.1.

Table 7.61. 4-bit LUT Truth Table of Standard Logic Gates

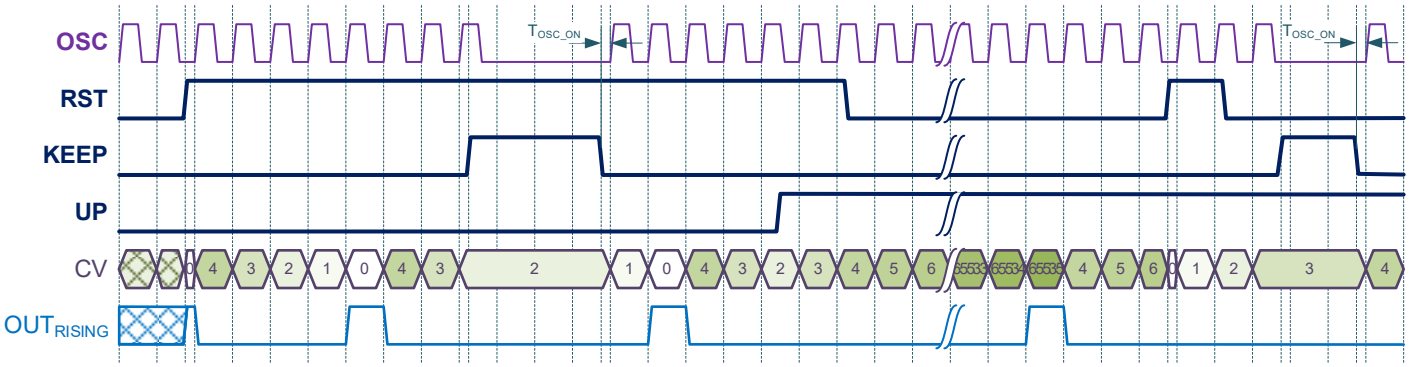
Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1



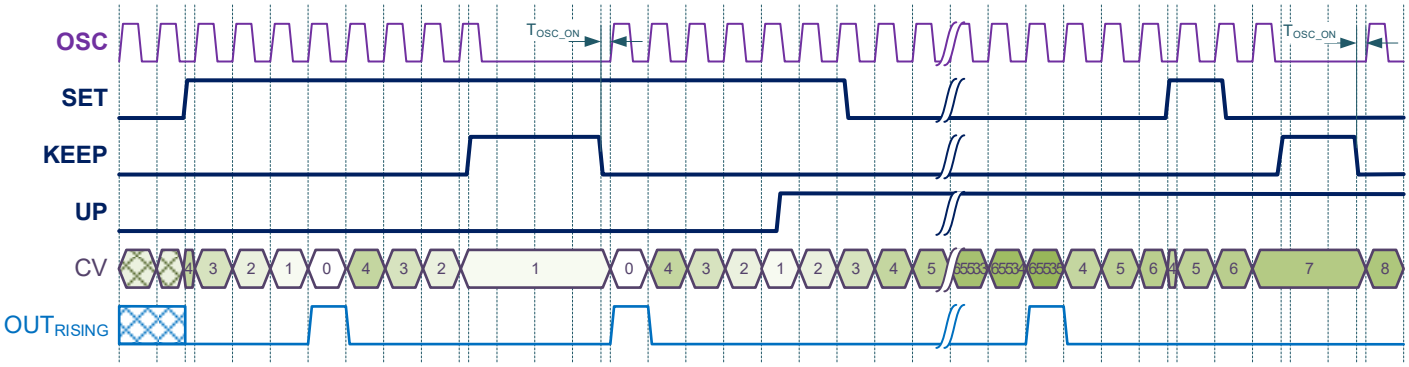
a) Rising Reset, Forced OSC



b) Rising Set, Forced OSC



c) Rising Reset, Auto OSC



d) Rising Set, Auto OSC

Figure 7.15. Up/Down Counter Timing Diagram (Control Data: 4)

7.7.1. MF22 (4-bit LUT0/16-bit TMR6 (WS)) Macrocells

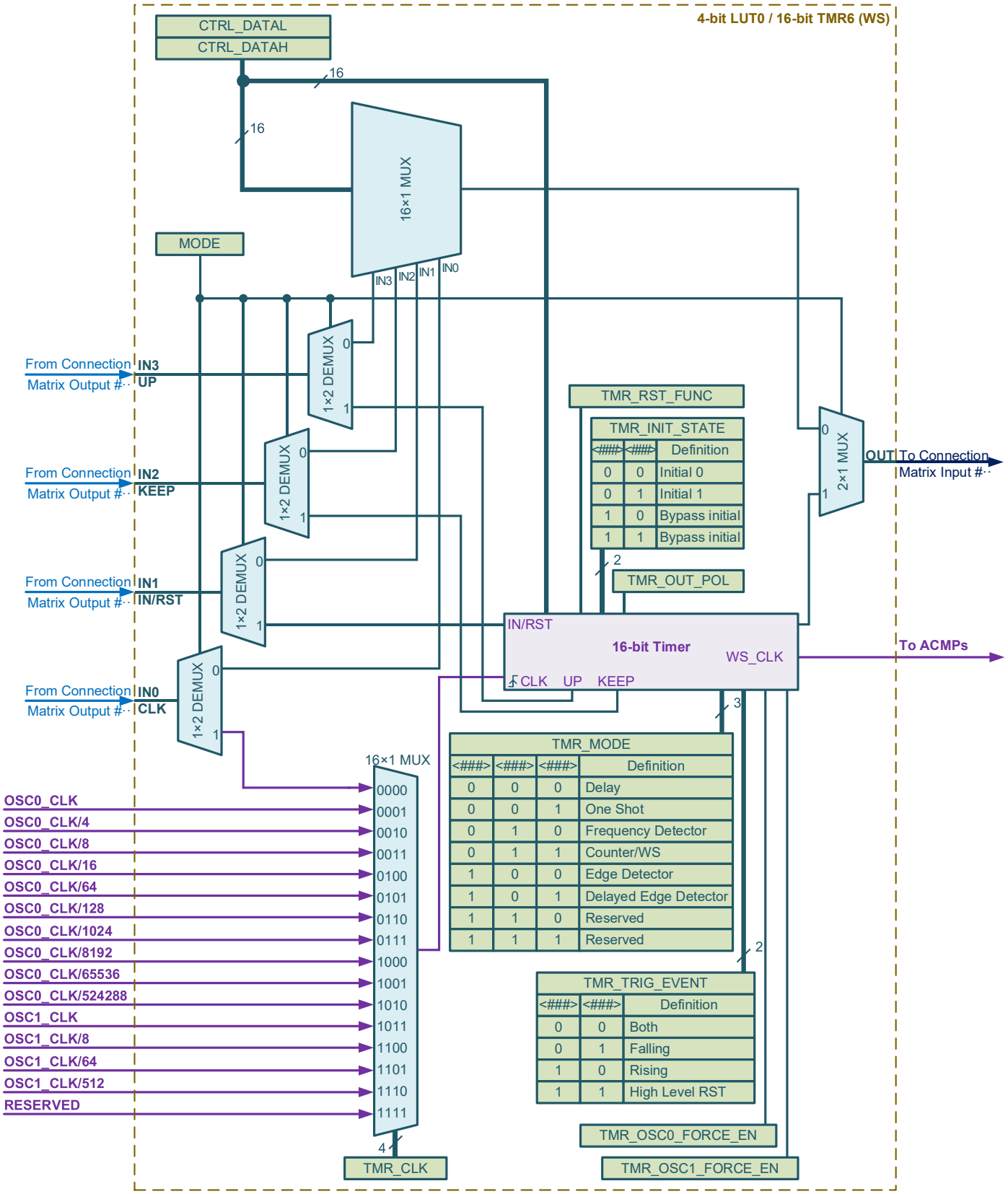
The MF macrocell in addition to the common operation modes can be used as a Wake&Sleep (WS) Controllers for ACMPs, what allows to reduce the ACMPs power consumption by turning on the ACMP only for a short period of time making measurement and turn off the ACMPs.
To control ACMPs with WS macrocell the following configuration should be performed:

- ACMP Power Up Input from matrix is HIGH (for desired ACMP);
- SET WS_EN register of desired ACMP;
- TMR6 should be set to Counter/Wake&Sleep function;
- RESET IN of WS is LOW in case MF22_CONF0_TMR_TRIG_EVENT set to High level reset.

The customer selects a period of time while the ACMPs are sleeping with Control Data of the TMR6 (1…65535). The ACMP state (High or Low) can be updated during Wake Time and Latch for sleeping time.

Schematic diagram of MF22 (4-bit LUT0/TMR6 (WS)) macrocell is shown on Figure 7.16.

Note 7.53: For the WS function the period of the input clock should be selected greater than ACMP Power On Time (t_{START}).



MF#	IN0/CLK	IN1/IN/RST	IN2/KEEP	IN3/UP	OUT
MF22 (4-bit LUT0/16-bit TMR6(WS))	CMO65	CMO66	CMO67	CMO68	CMI27

Figure 7.16. MF22 (4-bit LUT0/TMR6 (WS))

Table 7.62. MF22 (4-bit LUT0/TMR6 (WS)) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF22 (4-bit LUT0/TMR6 (WS))				
0x6800	<0>	MF22_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter/Wake&Sleep 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
0x6801	<3:0>	MF22_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.54) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>		TMR_RST_FUNC	Timer reset counted value functionality: 0: Reset to 0 1: Set to control data
0x6802	<7:0>	MF22_CTRL_DATAL		MF low byte of control data
0x6803	<7:0>	MF22_CTRL_DATAH		MF high byte of control data

Note 7.54 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 4-bit LUT0 uses 16-bit register to define its output function (see Table 7.63).

Table 7.63. 4-bit LUT0 Truth Table

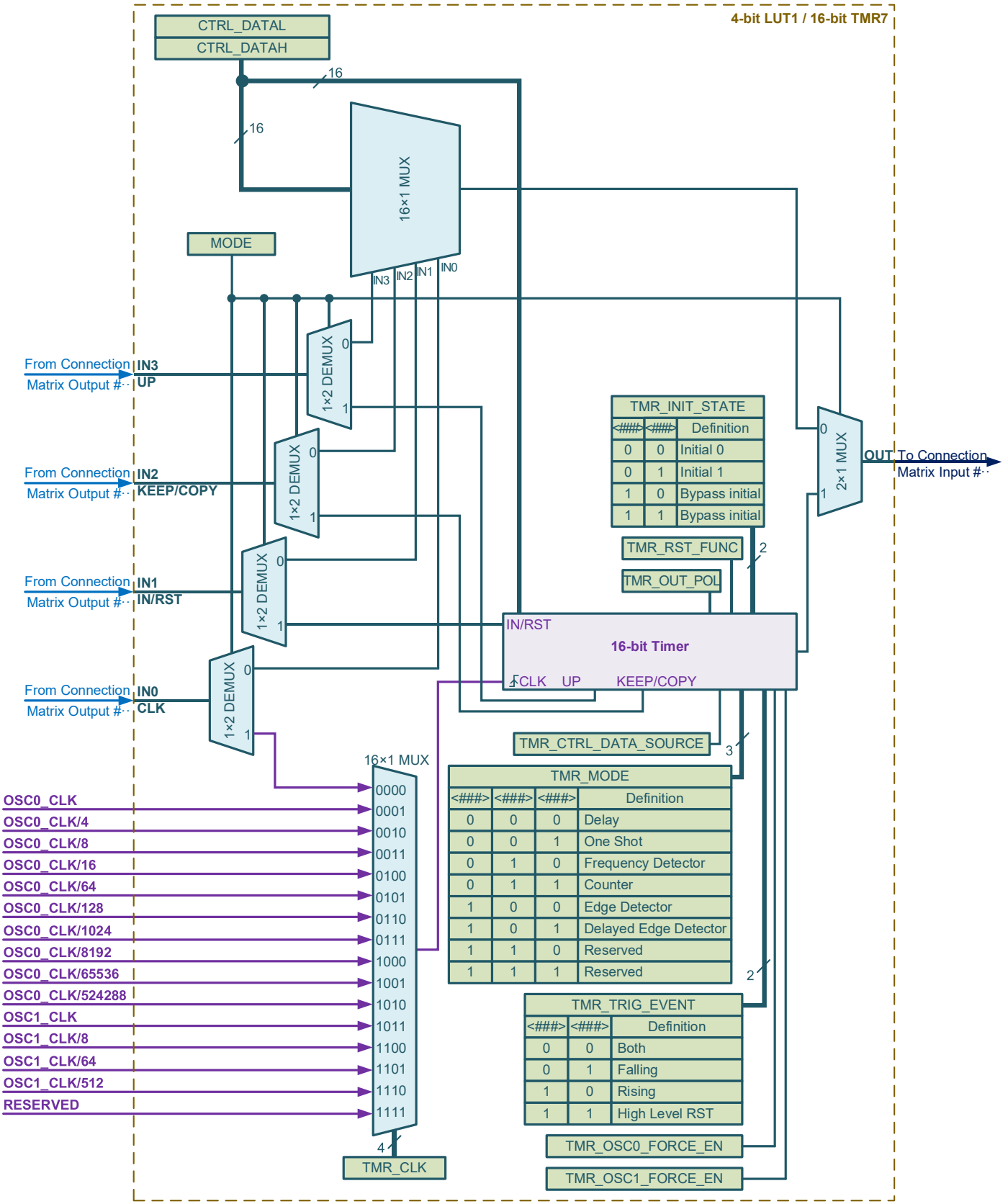
IN3	IN2	IN1	IN0	OUT	
0	0	0	0	MF22_CTRL_DATAL<0>	LSB
0	0	0	1	MF22_CTRL_DATAL<1>	
0	0	1	0	MF22_CTRL_DATAL<2>	
0	0	1	1	MF22_CTRL_DATAL<3>	
0	1	0	0	MF22_CTRL_DATAL<4>	
0	1	0	1	MF22_CTRL_DATAL<5>	
0	1	1	0	MF22_CTRL_DATAL<6>	
0	1	1	1	MF22_CTRL_DATAL<7>	
1	0	0	0	MF22_CTRL_DATAH<0>	
1	0	0	1	MF22_CTRL_DATAH<1>	
1	0	1	0	MF22_CTRL_DATAH<2>	
1	0	1	1	MF22_CTRL_DATAH<3>	
1	1	0	0	MF22_CTRL_DATAH<4>	
1	1	0	1	MF22_CTRL_DATAH<5>	
1	1	1	0	MF22_CTRL_DATAH<6>	
1	1	1	1	MF22_CTRL_DATAH<7>	MSB

7.7.2. MF23 (4-bit LUT1/16-bit TMR7)

This MF23 macrocell in addition to the common operation modes has a unique feature that allows to load the Counted Value of the MF23 (TMR6) to its Control Data registers by the rising edge on the COPY input. The COPY input is shared with the KEEP signal (defined by register TMR_CTRL_DATA_SOURCE) and IN2 of the 4-bit LUT.

Please note that updated data in registers CTRL_DATAH and CTRL_DATAL isn't saved after the µASIC is powered down, i.e. after the device is powered up, the CTRL_DATAH and CTRL_DATAL are loaded from NVM.

Schematic diagram of MF23 (4-bit LUT1/16-bit TMR7) macrocell is shown on Figure 7.17.



MF#	IN0/CLK	IN1/IN/RST	IN2/KEEP/COPY	IN3/UP	OUT
MF23 (4-bit LUT1/16-bit TMR7)	CMO69	CMO70	CMO71	CMO72	CMI28

Figure 7.17. 4-bit LUT1/16-bit TMR7

Table 7.64. MF23 (4-bit LUT1/16-bit TMR7) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF23 (4-bit LUT1/16-bit TMR7)				
0x6900	<0>	MF23_CONF0	MODE	MF mode: 0: LUT 1: Timer
	<3:1>		TMR_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
	<5:4>		TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
	<7:6>		TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
0x6901	<3:0>	MF23_CONF1	TMR_CLK	CLK source: 0000: External CLK 0001: OSC0 0010: OSC0/4 0011: OSC0/8 0100: OSC0/16 0101: OSC0/64 0110: OSC0/128 0111: OSC0/1024 1000: OSC0/8192 1001: OSC0/65536 1010: OSC0/524288 1011: OSC1 (Note 7.55) 1100: OSC1/8 1101: OSC1/64 1110: OSC1/512 1111: Reserved
	<4>		TMR_OSC0_FORCE_EN	Force OSC0 by timer: 0: Disable 1: Enable
	<5>		TMR_OSC1_FORCE_EN	Force OSC1 by timer: 0: Disable 1: Enable
	<6>		TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
	<7>		TMR_RST_FUNC	Timer reset counted value functionality: 0: Reset to 0 1: Set to control data
0x6902	<0>	MF23_CONF2	TMR_CTRL_DATA_SOURCE	Control data source: 0: Updated by NVM 1: Updated by counted value of TMR6
	<7:1>			Reserved
0x6903	<7:0>	MF23_CTRL_DATAL		MF low byte of control data
0x6904	<7:0>	MF23_CTRL_DATAH		MF high byte of control data

Note 7.55 When using OSC1 as a timer clock source, PRESCALER_MAIN in OSC1_CONF (0x9100) should be set to 0b01 (1/2), 0b10 (1/4), or 0b11 (1/8) for reliable timer operation (Table 10.4).

The 4-bit LUT1 uses 16-bit register to define its output function (see Table 7.65).

Table 7.65. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	MF23_CTRL_DATAL<0>	LSB
0	0	0	1	MF23_CTRL_DATAL<1>	
0	0	1	0	MF23_CTRL_DATAL<2>	
0	0	1	1	MF23_CTRL_DATAL<3>	
0	1	0	0	MF23_CTRL_DATAL<4>	
0	1	0	1	MF23_CTRL_DATAL<5>	
0	1	1	0	MF23_CTRL_DATAL<6>	
0	1	1	1	MF23_CTRL_DATAL<7>	
1	0	0	0	MF23_CTRL_DATAH<0>	
1	0	0	1	MF23_CTRL_DATAH<1>	
1	0	1	0	MF23_CTRL_DATAH<2>	
1	0	1	1	MF23_CTRL_DATAH<3>	
1	1	0	0	MF23_CTRL_DATAH<4>	
1	1	0	1	MF23_CTRL_DATAH<5>	
1	1	1	0	MF23_CTRL_DATAH<6>	
1	1	1	1	MF23_CTRL_DATAH<7>	MSB

7.8. MF (4-bit LUT/16-bit RPGEN) Macrocell

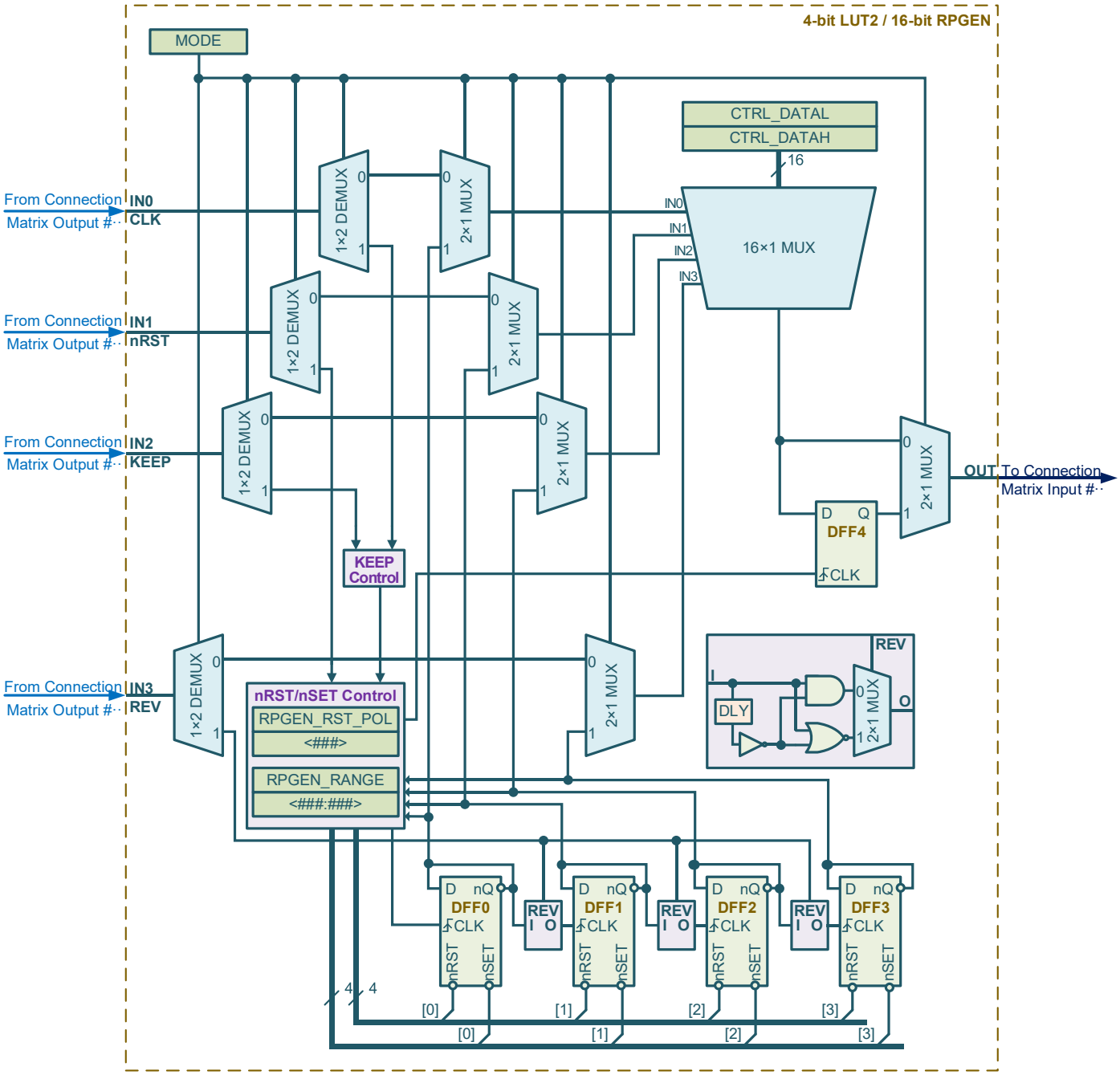
The macrocell has the capability to serve as a Look Up Table (LUT) or Reversible Programmable Pattern Generator (RPGEN).

When the MF macrocell is used as LUT, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.66.

When the macrocell is used as a Reversible Programmable Pattern Generator (RPGEN), the macrocell outputs pattern. There are four inputs for RPGEN: CLK, nRST (it can function as RST), KEEP (this signal pauses the functionality of RPGEN) and REV (reverse the movement of the pattern). See Figure 7.18 and Figure 7.19.

Table 7.66. 4-bit LUT Truth Table of Standard Logic Gates

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1



MF#	IN0/CLK	IN1/RST	IN2/KEEP	IN3/REV	OUT
MF24 (4-bit LUT2/16-bit RPGEN)	CMO73	CMO74	CMO75	CMO76	CMI32

Figure 7.18. MF24 (4-bit LUT2/16-bit RPGEN)

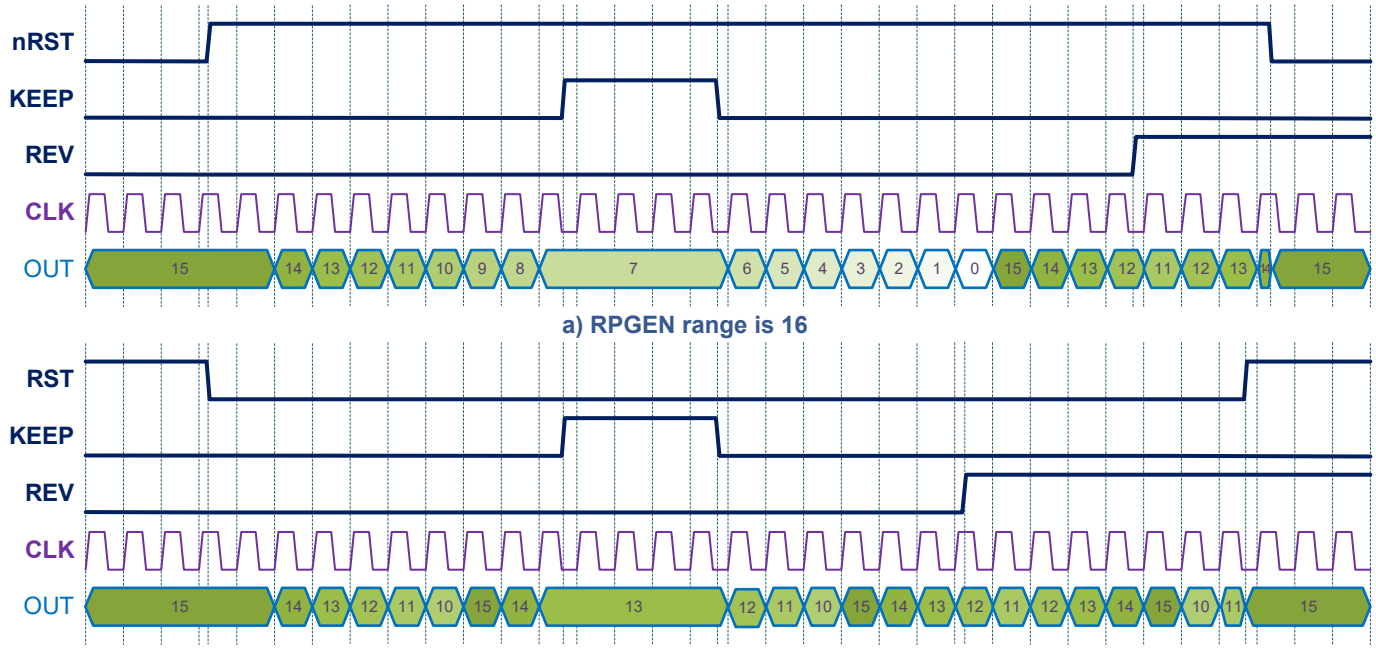


Figure 7.19. Timing diagrams of 16-bit RPGEN

7.8.1. MF24 (4-bit LUT2/16-bit RPGEN)

MF24 registers are listed in Table 7.67.

Table 7.67. MF24 (4-bit LUT2/16-bit RPGEN) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF24 (4-bit LUT2/16-bit RPGEN)				
0x6A00	<0>	MF24_CONF	MODE	MF mode: 0: LUT 1: RPGEN
	<1>		RPGEN_RST_POL	RPGEN reset polarity: 0: nRST 1: RST
	<2>			Reserved
	<3>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
	<7:4>		RPGEN_RANGE	RPGEN range: 0000: 1 0001: 2 0010: 3 0011: 4 0100: 5 0101: 6 0110: 7 0111: 8 1000: 9 1001: 10 1010: 11 1011: 12 1100: 13 1101: 14 1110: 15 1111: 16
0x6A01	<7:0>	MF24_CTRL_DATAL		MF low byte of control data
0x6A02	<7:0>	MF24_CTRL_DATAH		MF high byte of control data

The 4-bit LUT2 uses 16-bit register to define its output function (see Table 7.68).

Table 7.68. 4-bit LUT2 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	MF24_CTRL_DATAL<0>	LSB
0	0	0	1	MF24_CTRL_DATAL<1>	
0	0	1	0	MF24_CTRL_DATAL<2>	
0	0	1	1	MF24_CTRL_DATAL<3>	
0	1	0	0	MF24_CTRL_DATAL<4>	
0	1	0	1	MF24_CTRL_DATAL<5>	
0	1	1	0	MF24_CTRL_DATAL<6>	
0	1	1	1	MF24_CTRL_DATAL<7>	
1	0	0	0	MF24_CTRL_DATAH<0>	
1	0	0	1	MF24_CTRL_DATAH<1>	
1	0	1	0	MF24_CTRL_DATAH<2>	
1	0	1	1	MF24_CTRL_DATAH<3>	
1	1	0	0	MF24_CTRL_DATAH<4>	
1	1	0	1	MF24_CTRL_DATAH<5>	
1	1	1	0	MF24_CTRL_DATAH<6>	
1	1	1	1	MF24_CTRL_DATAH<7>	MSB

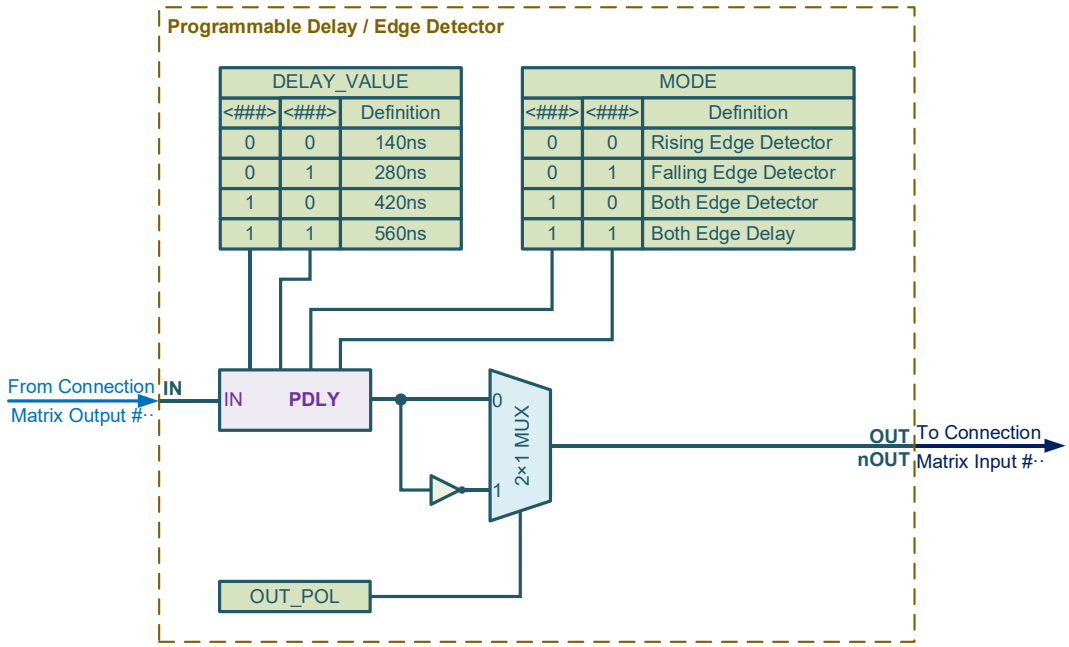
7.9. MF (PDLY/Edge Detector) Macrocell

The AM1U1514 has a macrocell that can serve as programmable delay (PDLY) or as edge detector.

In the PDLY mode the macrocell serves as both edge delay with four selectable delay value T_{ADJ}: 140 ns, 280 ns, 420 ns, 560 ns. If input signal is shorter than the delay value, the signal does not propagate to the output and is filtered out.

In the Edge Detector mode, the macrocell generates a high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The pulse width value (T_{WIDTH}) is configurable (140 ns, 280 ns, 420 ns, 560 ns). See the timing diagrams below for further information (Figure 7.21).

The output polarity of the macrocell is configurable and can be selected as non-inverted or inverted.



MF#	IN	OUT
MF25 (PDLY/Edge Detector)	CMO77	CMI33

Figure 7.20. MF25 (PDLY/Edge Detector)

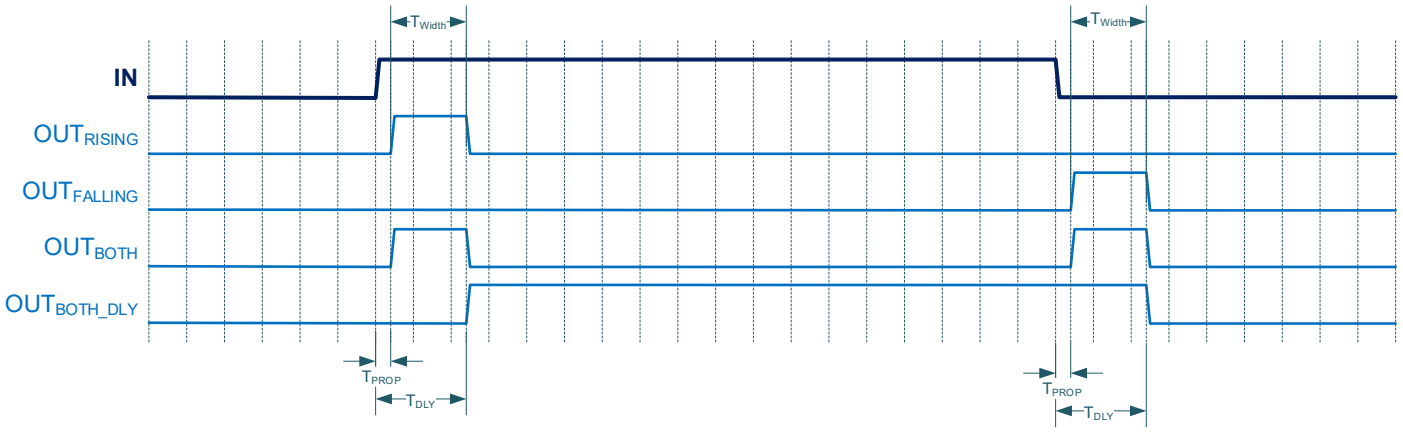


Figure 7.21. Edge Detector Output

7.9.1. MF25 (PDLY/Edge Detector)

MF25 registers are listed in Table 7.69.

Table 7.69. MF25 (PDLY/Edge Detector) Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
MF25 (PDLY/Edge Detector)				
0x6B00	<1:0>	MF25_CONF	MODE	MF mode: 00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
	<2>		OUT_POL	Output polarity: 0: OUT 1: nOUT
	<4:3>		DELAY_VALUE	Delay value: 00: 140ns 01: 280ns 10: 420ns 11: 560ns
	<7:5>			Reserved

8. Memory Architecture

The Memory of µASIC consists of two main parts: non-volatile memory (NVM) and registers. The configuration of the µASIC is stored in the NVM and is loaded to the volatile registers, during device power up. The registers values define macrocells configuration, matrix connections setting (signal routing), IO configuration etc., that allows to get the desired functionality for user's application (see Figure 8.1).

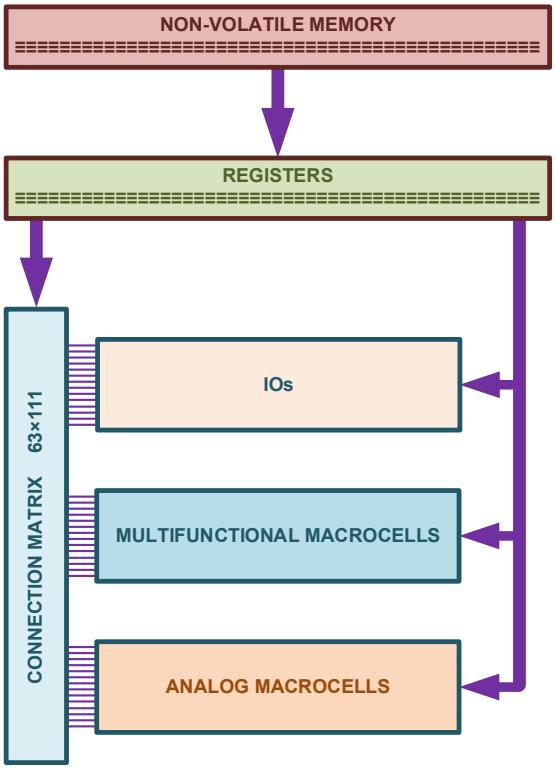


Figure 8.1. Memory Architecture

9. Data Protection

The AM1U1514 has two data protection features, CRC-8 and CRV that are enabled by SYS_SECURITY_CTRL (Table 9.1).

Table 9.1. Security Control Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
Security Control				
0x1200	<0>	SYS_SECURITY_CTRL	CRC_EN	CRC verification: 0: Disable 1: Enable
	<1>		CRV_EN	Continuous register verification: 0: Disable 1: Enable
	<4:2>			Reserved
	<5>		CRV_B	CRV bit. Value is HIGH
	<6>			Reserved
	<7>		CRV_B	CRV bit. Value is LOW
0x1201	<7:0>	SYS_SECURITY_CRC		CRC ($x^8+x^6+x^3+1$)

9.1. CRC-8

Validity of correct NVM programming and NVM loading to the registers is checked by CRC-8. If the CRC-8 is Enabled and no errors is detected the AM1U1514 powers up, otherwise the chip will be restarted. CRC polynomial is $x^8 + x^6 + x^3 + 1$.

9.2. CRV

Continuous Registers Verification (CRV) is provided by a continuous comparison of the dedicated register bits spread all over the memory with hardcoded value 32'b11000110101100100110100110111001. If the comparison shows a mismatch the µASIC automatically restarts.

10. Oscillators (OSCs)

10.1. Oscillators Overview

AM1U1514 has two internal oscillators that allow to cover a variety of application:
- OSC0 with two selectable output frequencies 25 kHz or 2 MHz
- OSC1 with output frequency 25 MHz

Both OSCs macrocells can be sourced either from internal oscillator or by external frequency from IO13 for OSC0.

The OSC0 has two prescaler stages that gives user flexibility for introducing clock signals on the Connection Matrix Input lines. The first stage (main prescaler) allows to divide the fundamental frequency by **/1**, **/2**, **/4** or **/8**. The two independent second stage prescaler allow to divide the frequency from the first stage divider by **/1**, **/2** or **/4**, **/8**, **/16, /32, /64**, **/128** or **/256**, and outputs this frequency on the Connection Matrix Input #29 and #30 (See Figure 10.1 for more details).

The OSC1 has one prescaler stages that gives user flexibility for introducing clock signal on the Connection Matrix Input #31. The fundamental frequency can be divided by **/1**, **/2**, **/4** or **/8** (See Figure 10.2 for more details).

Each oscillator has three power states of operation (see Table 10.1). The flow of turning on the oscillator is started from OFF state, then it goes to IDLE state and last is ON state in which frequency appear on the oscillator output.

Table 10.1. Oscillator power states

State	Description
OFF state	The oscillator is fully shut down and consumes the minimum amount of current (less than 1nA). The power on time of the oscillator is longer compare to the power on from the IDLE state (see Table 4.11, Table 4.15, Table 4.19). The oscillator stays in this state when it is not turned on by timers or control input, and Power On Time is selected as normal.
IDLE state	The power consumption is higher compared to the OFF state and depends on the type of oscillator (see Table 4.5). The oscillator is ready to operate and power on time is within 1 clock cycle of the oscillator.
ON state	The oscillator consumes its active current and frequency is generated on the oscillator output (see Table 4.5)

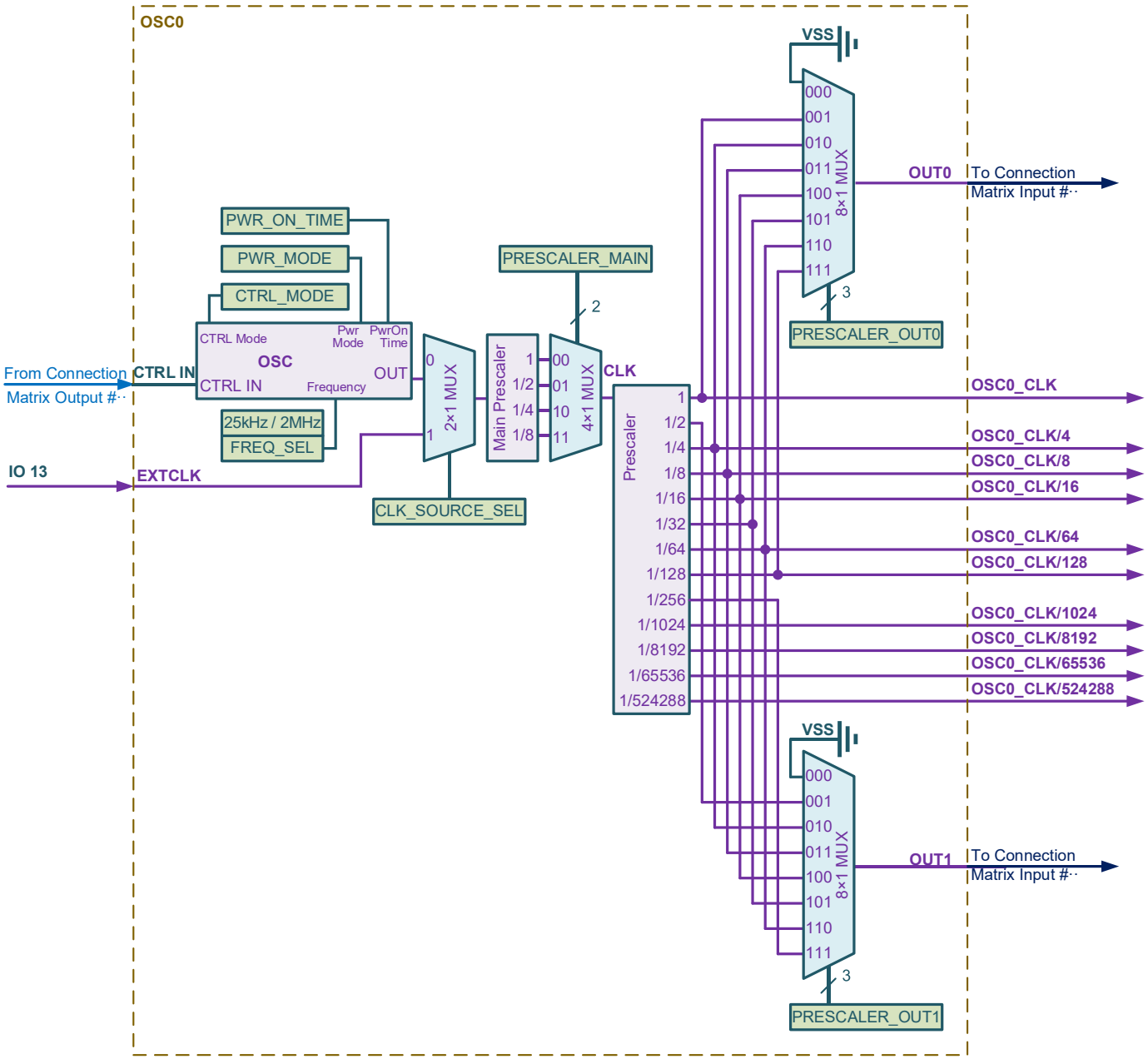
Each oscillators have three settings that allow to choose appropriate mode of operation (see Table 10.2).

Table 10.2. Oscillator setting

Setting	Option	Description
Power On Time	Normal	The oscillator power on time is normal (see Table 4.11, Table 4.15, Table 4.19). When the oscillator is turned off it stays in the OFF state.
	Fast	The oscillator power on time fast, within 1 clock cycle (see Table 4.11, Table 4.15, Table 4.19). When the oscillator is turned off it stays in the IDLE state.
Control Input Mode	Power down	High level of CTRL IN turns off the oscillator. The low level of CTRL IN doesn't affect the operation of the oscillator.
	Force on	HIGH level of CTRL IN turns on the oscillator. The low level of CTRL IN doesn't affect the operation of the oscillator.
Power Mode	Auto power on	The oscillator is turned on when any of timers require it, or control input signal force it (Note 10.1).
	Forced power on	The oscillator is turned on when part is powered on and control input signal doesn't shut down it.

Note 10.1 Power control signal has the highest priority.

10.2. OSC0 (25kHz/2MHz)



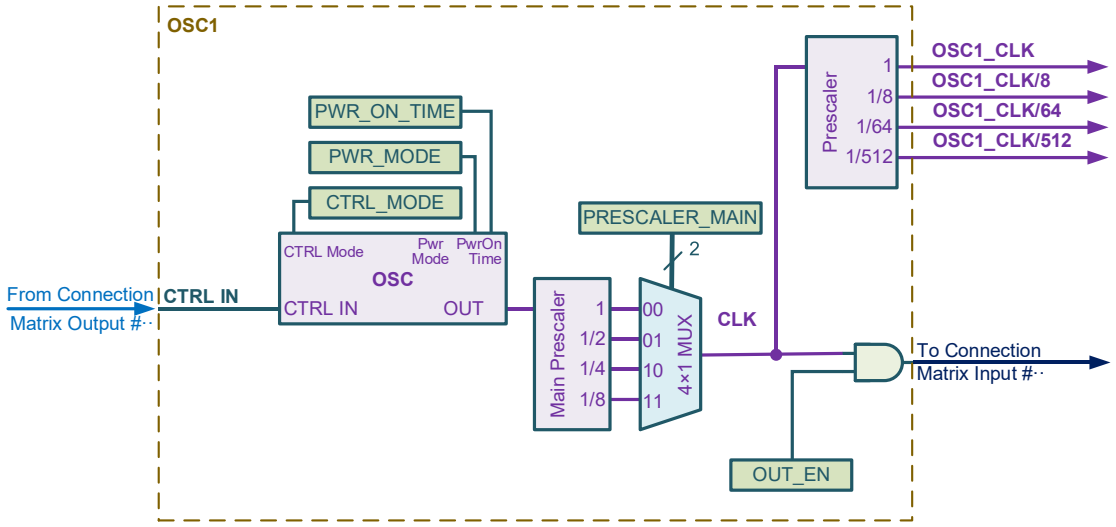
Oscillator	CTRL_IN	OUT0	OUT1
OSC0	CMO79	CMI29	CMI30

Figure 10.1. OSC0(25 kHz/2 MHz) Block Diagram

Table 10.3. OSC0 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
OSC0				
0x9000	<0>	OSC0_CONF0	FREQ_SEL	Frequency: 0: 25kHz 1: 2MHz
	<1>		CTRL_MODE	Control Input mode control: 0: Power down 1: Force on
	<2>		PWR_MODE	Power mode: 0: Auto power on 1: Forced power on
	<3>		PWR_ON_TIME	Power on time: 0: Normal 1: Fast
	<4>		CLK_SOURCE_SEL	Clock source: 0: Inner oscillator 1: External CLK
	<7:5>			Reserved
0x9001	<1:0>	OSC0_PRESCALER	MAIN	Main prescaler: 00: 1 01: 1/2 10: 1/4 11: 1/8
	<4:2>		OUT0	OUT0 prescaler: 000: OUT0_DISABLE 001: OSC0_CLK 010: OSC0_CLK/4 011: OSC0_CLK/8 100: OSC0_CLK/16 101: OSC0_CLK/32 110: OSC0_CLK/64 111: OSC0_CLK/128
	<7:5>		OUT1	OUT1 prescaler: 000: OUT1_DISABLE 001: OSC0_CLK/2 010: OSC0_CLK/4 011: OSC0_CLK/8 100: OSC0_CLK/16 101: OSC0_CLK/32 110: OSC0_CLK/64 111: OSC0_CLK/256

10.3. OSC1 (25MHz)



Oscillator	CTRL_IN	OUT
OSC1	CMO80	CMI31

Figure 10.2. OSC1(25 MHz) Block Diagram

Table 10.4. OSC1 Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
OSC1				
0x9100	<0>	OSC1_CONF0	PWR_ON_TIME	Power on time: 0: Normal 1: Fast
	<1>		CTRL_MODE	Control Input mode control: 0: Power down 1: Force on
	<2>		PWR_MODE	Power mode: 0: Auto power on 1: Forced power on
	<3>			Reserved
	<5:4>		PRESCALER_MAIN	Main Prescaler: 00: 1 01: 1/2 10: 1/4 11: 1/8
	<6>		OUT_EN	Enable OUT to Connection Matrix: 0: Disable 1: Enable
	<7>			Reserved

11. Analog Comparators (ACMP)

The µASIC has 4 Analog Comparator macrocells (ACMP), that can be used to compare the voltage of two analog inputs (IN+ and IN-), with a digital output going to the matrix connection indicating which input voltage is higher. When the voltage at IN+ input is higher than voltage at IN- the digital output is HIGH and vice versa.

The ACMP also has PWR ON input, coming from the connection matrix, and used to power on/off the ACMP. This allows to control the ACMP power on/off state from the connection matrix. The output of the ACMP is LOW when the ACMP PWR ON signal is LOW. Also, there is one more input which is coming from the TMR6 output, when the ACMP is configured for the Wake&Sleep (WS) mode. It allows to reduce average current consumption of the part by switching on/off periodically the ACMP. In the WS mode the ACMP output will keep it previous value during power off time.

PWR ON = 1 => ACMP is powered on.
PWR ON = 0 => ACMP is powered off.

The ACMP output remains low during ACMP start up time (see Table 4.21) and then becomes valid.
For each ACMP can be enabled low power mode that reduces the total current consumption of the ACMP, by reducing the bandwidth of the ACMP.

ACMP IN+ and IN- can be sourced with a variety of external and internal source with a recommended voltage range IN+ = 0…VDD, IN- = 0…VDD-0.3V. Also, there is a selectable gain stage for the IN+ input, that allows to select one of the following gains: 1.00×, 0.50×, 0.33×, 0.25×. Each ACMP has an optional input buffer on the IN+ input, which can be used along with the gain stage to increase IN+ input resistance (see Table 4.21 for R_{SIN}). However, the input buffer increases an input offset voltage and current consumption of the ACMP.

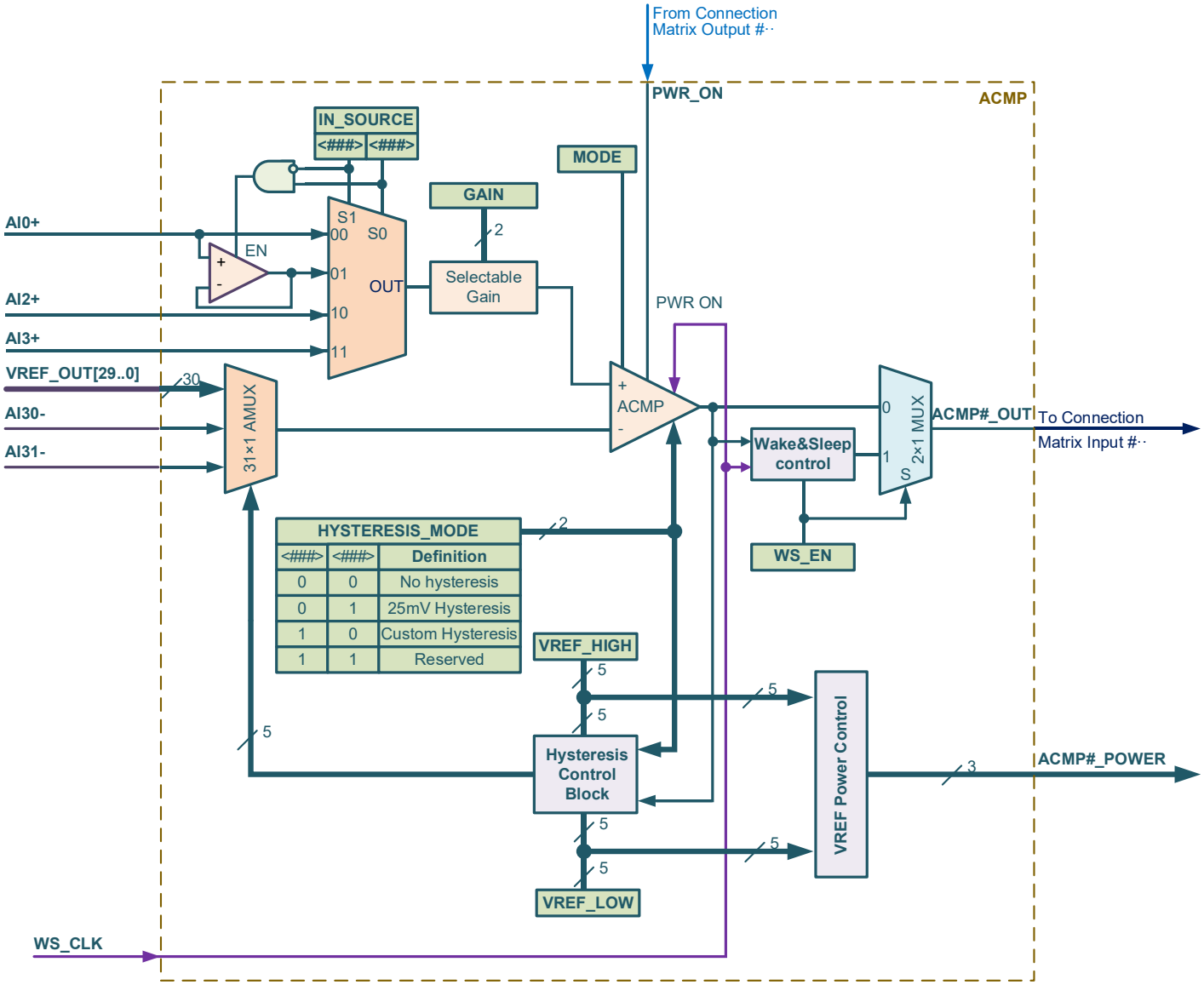
ACMP has three selectable hysteresis modes:

- No hysteresis;
- 25mV Hysteresis. This mode set hysteresis 25mV that can be used either for internal or external reference. The high threshold is VREF + hysteresis/2 and the low threshold is VREF – hysteresis/2;
- Custom Hysteresis. In this mode there is a possibility to directly select low to high (VREFH) and high to low (VREFL) thresholds. This mode functions only with an internal VREF used.

IO6, IO10 can be used as a common negative input for all ACMPs.

Configurations of ACMPs are shown in Table 11.1, Table 11.3, Table 11.5 and Table 11.7.

11.1. ACMP Block Diagram



ACMP#	AI0+	AI2+	AI3+	AI30-	AI31-	PWR_ON	ACMP#_OUT
ACMP0	IO5	TS_OUT	VDD	IO10	IO6	CMO81	CMI43
ACMP1	IO7	ACMP0 IN+	IO2	IO10	IO6	CMO82	CMI44
ACMP2	IO8	ACMP0 IN+	IO3	IO6	IO10	CMO83	CMI45
ACMP3	IO11	ACMP0 IN+	ACMP2 IN+	IO6	IO10	CMO84	CMI46

Figure 11.1. ACMP Block Diagram

11.2. ACMP0 Register Setting

Table 11.1 ACMP0 Register Setting

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
ACMP0				
0x9200	<1:0>	ACMP0_CONF	IN_SOURCE	IN+ source: 00: IO5 01: Buffered IO5 10: Temperature sensor out 11: VDD
	<3:2>		GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
	<5:4>		HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 11.1) 01: 25mV (see Note 11.1) 10: Custom hysteresis 11: Reserved
	<6>		MODE	Mode: 0: High speed 1: Low power (see Note 11.2)
	<7>		WS_EN	Wake&Sleep: 0: Disable 1: Enable
0x9201	<4:0>	ACMP0_VREFL	VREFL	High to Low threshold: see Table 11.2
	<7:5>			Reserved
0x9202	<4:0>	ACMP0_VREFH	VREFH	Low to High threshold: see Table 11.2
	<5>		CRV_B	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
	<7:6>			Reserved

Note 11.1 In this hysteresis mode, ACMP0_VREFH is used as voltage reference.

Note 11.2 With low current consumption (Low Power Mode), input noise suppression is also achieved by lowering the input bandwidth.

Table 11.2. ACMP0 Voltage Reference Selection

Selection Registers <4:0>	VREF	Selection Registers <4:0>	VREF
00000	50mV	10000	850mV
00001	100mV	10001	900mV
00010	150mV	10010	950mV
00011	200mV	10011	1000mV
00100	250mV	10100	1050mV
00101	300mV	10101	1100mV
00110	350mV	10110	1150mV
00111	400mV	10111	1200mV
01000	450mV	11000	VDD/2
01001	500mV	11001	VDD/3
01010	550mV	11010	VDD/4
01011	600mV	11011	TS_OUT
01100	650mV	11100	EXT_VREF (IO10)
01101	700mV	11101	EXT_VREF (IO10)/2
01110	750mV	11110	EXT_VREF (IO10)
01111	800mV	11111	EXT_VREF (IO6)

11.3. ACMP1 Register Setting

Table 11.3 ACMP1 Register Setting

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
ACMP1				
0x9300	<1:0>	ACMP1_CONF	IN_SOURCE	IN+ source: 00: IO7 01: Buffered IO7 10: ACMP0 IN+ 11: IO2
	<3:2>		GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
	<5:4>		HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 11.3) 01: 25mV (see Note 11.3) 10: Custom hysteresis 11: Reserved
	<6>		MODE	Mode: 0: High speed 1: Low power (see Note 11.4)
	<7>		WS_EN	Wake&Sleep: 0: Disable 1: Enable
0x9301	<4:0>	ACMP1_VREFL	VREFL	High to Low threshold: see Table 11.4
	<7:5>			Reserved
0x9302	<4:0>	ACMP1_VREFH	VREFH	Low to High threshold: see Table 11.4
	<7:5>			Reserved

Note 11.3 In this hysteresis mode, ACMP1_VREFH is used as voltage reference.

Note 11.4 With low current consumption (Low Power Mode), input noise suppression is also achieved by lowering the input bandwidth.

Table 11.4. ACMP1 Voltage Reference Selection

Selection Registers <4:0>	VREF	Selection Registers <4:0>	VREF
00000	50mV	10000	850mV
00001	100mV	10001	900mV
00010	150mV	10010	950mV
00011	200mV	10011	1000mV
00100	250mV	10100	1050mV
00101	300mV	10101	1100mV
00110	350mV	10110	1150mV
00111	400mV	10111	1200mV
01000	450mV	11000	VDD/2
01001	500mV	11001	VDD/3
01010	550mV	11010	VDD/4
01011	600mV	11011	TS_OUT
01100	650mV	11100	EXT_VREF (IO10)
01101	700mV	11101	EXT_VREF (IO10)/2
01110	750mV	11110	EXT_VREF (IO10)
01111	800mV	11111	EXT_VREF (IO6)

11.4. ACMP2 Register Setting

Table 11.5 ACMP2 Register Setting

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
ACMP2				
0x9400	<1:0>	ACMP2_CONF	IN_SOURCE	IN+ source: 00: IO8 01: Buffered IO8 10: ACMP0 IN+ 11: IO3
	<3:2>		GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
	<5:4>		HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 11.3) 01: 25mV (see Note 11.3) 10: Custom hysteresis 11: Reserved
	<6>		MODE	Mode: 0: High speed 1: Low power (see Note 11.4)
	<7>		WS_EN	Wake&Sleep: 0: Disable 1: Enable
0x9401	<4:0>	ACMP2_VREFL	VREFL	High to Low threshold: see Table 11.6
	<7:5>			Reserved
0x9402	<4:0>	ACMP2_VREFH	VREFH	Low to High threshold: see Table 11.6
	<7:5>			Reserved

Note 11.5 In this hysteresis mode, ACMP2_VREFH is used as voltage reference.

Note 11.6 With low current consumption (Low Power Mode), input noise suppression is also achieved by lowering the input bandwidth.

Table 11.6. ACMP2 Voltage Reference Selection

Selection Registers <4:0>	VREF	Selection Registers <4:0>	VREF
00000	50mV	10000	850mV
00001	100mV	10001	900mV
00010	150mV	10010	950mV
00011	200mV	10011	1000mV
00100	250mV	10100	1050mV
00101	300mV	10101	1100mV
00110	350mV	10110	1150mV
00111	400mV	10111	1200mV
01000	450mV	11000	VDD/2
01001	500mV	11001	VDD/3
01010	550mV	11010	VDD/4
01011	600mV	11011	TS_OUT
01100	650mV	11100	EXT_VREF (IO10)
01101	700mV	11101	EXT_VREF (IO10)/2
01110	750mV	11110	EXT_VREF (IO6)
01111	800mV	11111	EXT_VREF (IO10)

11.5. ACMP3 Register Setting

Table 11.7 ACMP3 Register Setting

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
ACMP3				
0x9500	<1:0>	ACMP3_CONF	IN_SOURCE	IN+ source: 00: IO11 01: Buffered IO11 10: ACMP0 IN+ 11: ACMP2 IN+
	<3:2>		GAIN	IN+ gain: 00: 1.00× 01: 0.50× 10: 0.33× 11: 0.25×
	<5:4>		HYSTERESIS_MODE	Hysteresis mode: 00: No hysteresis (see Note 11.3) 01: 25mV (see Note 11.3) 10: Custom hysteresis 11: Reserved
	<6>		MODE	Mode: 0: High speed 1: Low power (see Note 11.4)
	<7>		WS_EN	Wake&Sleep: 0: Disable 1: Enable
0x9501	<4:0>	ACMP3_VREFL	VREFL	High to Low threshold: see Table 11.8
	<7:5>			Reserved
0x9502	<4:0>	ACMP3_VREFH	VREFH	Low to High threshold: see Table 11.8
	<7:5>			Reserved

Note 11.7 In this hysteresis mode, ACMP3_VREFH is used as voltage reference.

Note 11.8 With low current consumption (Low Power Mode), input noise suppression is also achieved by lowering the input bandwidth.

Table 11.8. ACMP3 Voltage Reference Selection

Selection Registers <4:0>	VREF	Selection Registers <4:0>	VREF
00000	50mV	10000	850mV
00001	100mV	10001	900mV
00010	150mV	10010	950mV
00011	200mV	10011	1000mV
00100	250mV	10100	1050mV
00101	300mV	10101	1100mV
00110	350mV	10110	1150mV
00111	400mV	10111	1200mV
01000	450mV	11000	VDD/2
01001	500mV	11001	VDD/3
01010	550mV	11010	VDD/4
01011	600mV	11011	TS_OUT
01100	650mV	11100	EXT_VREF (IO10)
01101	700mV	11101	EXT_VREF (IO10)/2
01110	750mV	11110	EXT_VREF (IO6)
01111	800mV	11111	EXT_VREF (IO10)

12. Voltage Reference (VREF)

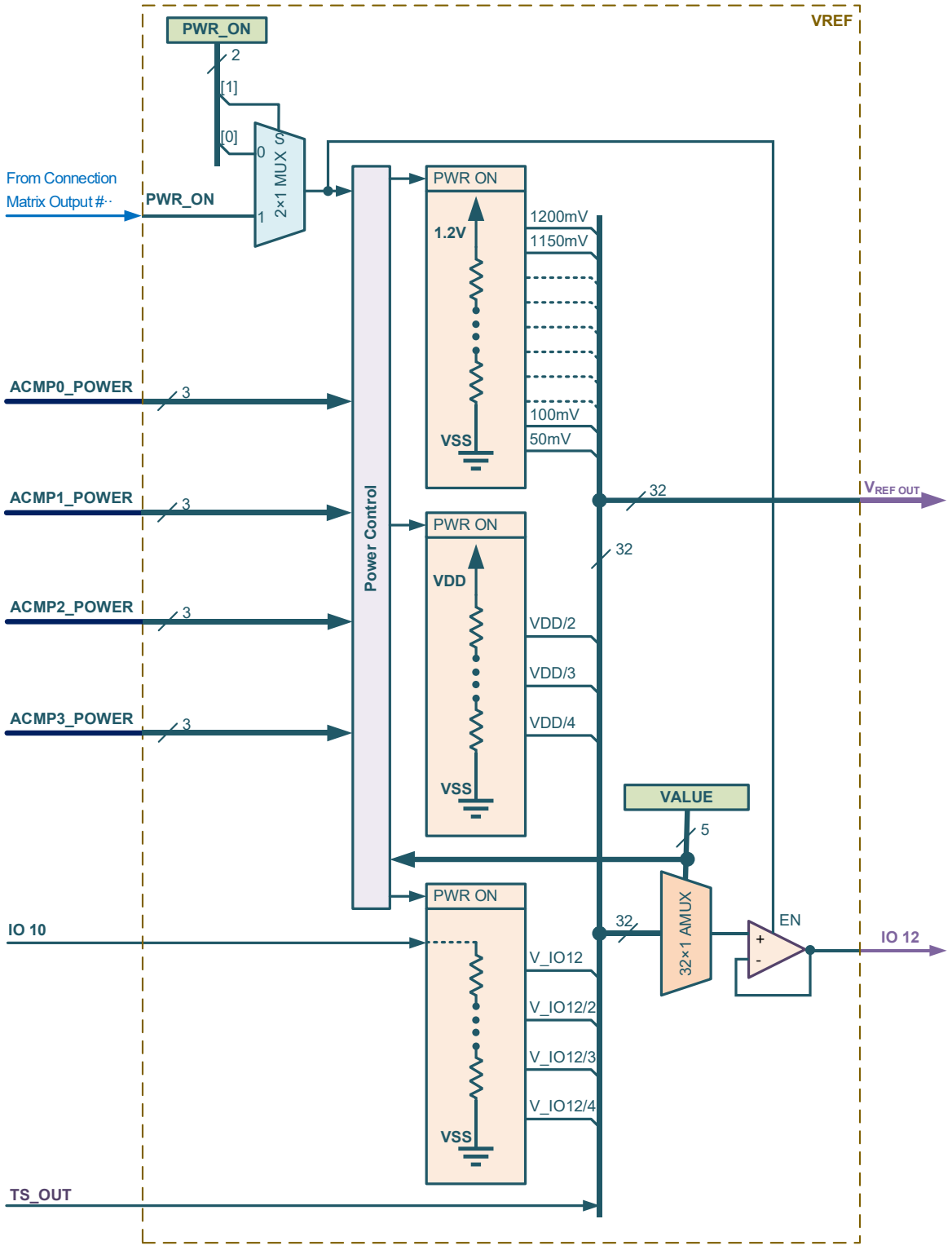
The µASIC has built-in Voltage Reference (VREF) Macrocell that provides a variety of selectable voltage levels to ACMPs (see Table 12.1). Also, the macrocell has an option to output reference voltage on IO12 (Table 12.2, Figure 12.1). The VREF macrocell has a selection of internally generated voltage references, temperature sensor output voltage, /2, /3 and /4 reference of V_{DD}, and externally supplied voltage reference from IO10, that also can be divided via voltage divider. The input impedance of the divider can be found in Table 4.22 (R_{VDD_DIV}, R_{EXT_DIV}).

Table 12.1. VREF Selection

Selection Registers <4:0>	VREF
00000	50mV
00001	100mV
00010	150mV
00011	200mV
00100	250mV
00101	300mV
00110	350mV
00111	400mV
01000	450mV
01001	500mV
01010	550mV
01011	600mV
01100	650mV
01101	700mV
01110	750mV
01111	800mV
10000	850mV
10001	900mV
10010	950mV
10011	1000mV
10100	1050mV
10101	1100mV
10110	1150mV
10111	1200mV
11000	VDD/2
11001	VDD/3
11010	VDD/4
11011	TS_OUT
11100	EXT_VREF (IO10)
11101	EXT_VREF (IO10)/2
11110	EXT_VREF (IO10)/3
11111	EXT_VREF (IO10)/4

Table 12.2 VREF Register Setting

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
VREF				
0x9600	<0>	VREF_CONF	PWR_ON	VREF output to IO12 power on: 00: Power Off 01: Power On 10: Controlled by Connection Matrix 11: Controlled by Connection Matrix
	<1>			
	<7:2>			Reserved
0x9601	<4:0>	VREF_IO_VALUE		VREF IO value: see Table 12.1
	<7:5>			Reserved



Voltage Reference	PWR_ON
VREF	CMO89 (shared with IO12 DIR and TS PWR_ON)

Figure 12.1. Voltage Reference Block Diagram

13. Analog Temperature Sensor

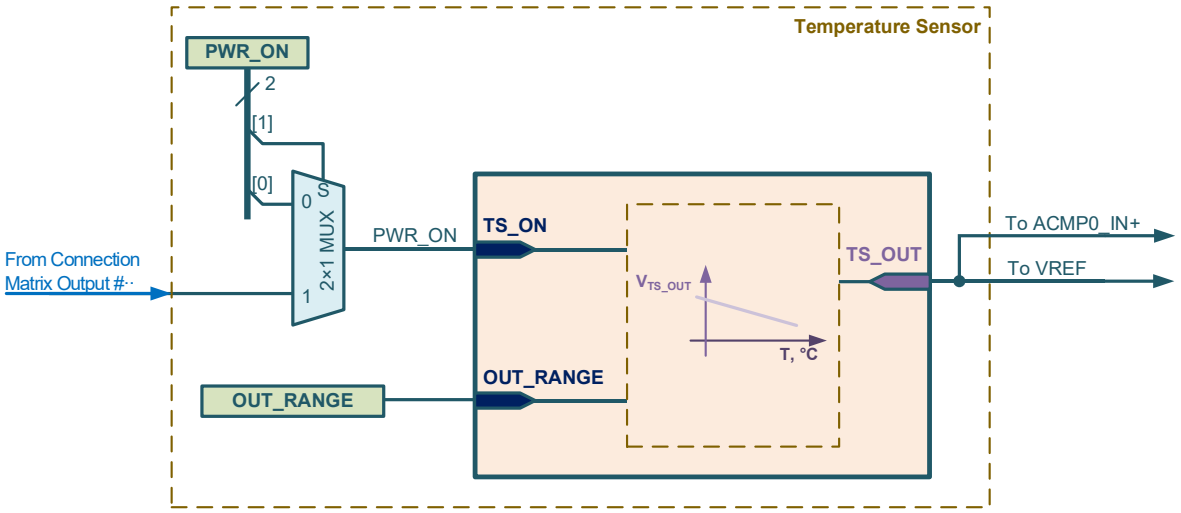
The µASIC has an Analog Temperature Sensor (TS), which output voltage is linearly-proportional to Centigrade temperature (Figure 13.1, Figure 13.2, Table 13.1). The TS output can be connected to the VREF and then route to IO12 or to ACMP0 IN+. The TS shares output with VREF.

The TS operation temperature range is -40°C to 85°C. The error does not exceed ±5°C in the whole temperature range. Refer to section 4.10. Analog Temperature Sensor (TS) Specifications for more detail.

The TS output voltage (mV) can be calculated by using the following formula:

$$V_{TS\ (Output\ range1)} = -2.74 \times T + 865.1;$$
$$V_{TS\ (Output\ range2)} = -3.15 \times T + 1071.4,$$

where T – current temperature, °C.



Temperature Sensor	PWR_ON
TS	CMO89 (shared with VREF PWR_ON and IO12 DIR)

Figure 13.1. Analog Temperature Sensor Block Diagram

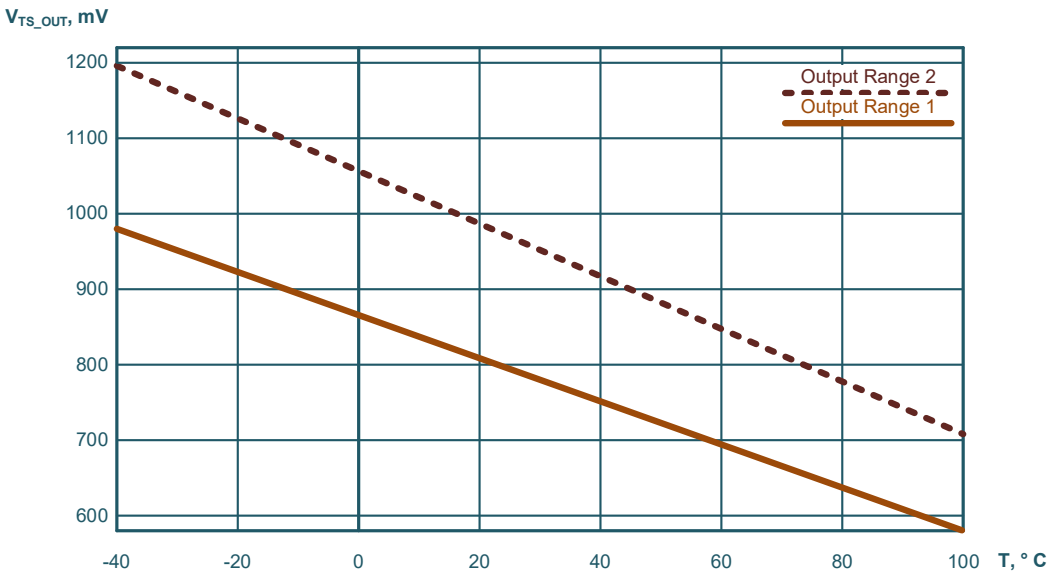


Figure 13.2. Analog Temperature Sensor Block Diagram

Table 13.1 Analog Temperature Sensor Register Setting

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
Analog Temperature Sensor				
0x9800	<0>	TEMP_SENS_CONF	PWR_ON	TS power on: 00: Power Off 01: Power On 10: Controlled by Connection Matrix 11: Controlled by Connection Matrix
	<1>			
	<2>		OUT_RANGE	Output range: 0: Output range1 (620mV…990mV) 1: Output range2 (750mV…1200mV)
	<7:3>			Reserved

14. 100µA Current Source

The µASIC has 100µA Current Source connected to IO7 (IN+ ACMP1) (Figure 14.1). The current source can be used either as standalone or together with the ACMP1 for various purpose. 100µA Current Source can be turned on by corresponding register (Table 14.1).

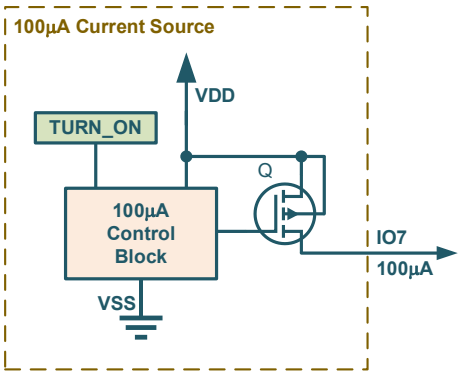


Figure 14.1. 100uA Current Source Block Diagram

Table 14.1 100µA Current Source Registers

Byte Address (type)	Register Bit Address	Register Name	Bit Name	Register Definition
100µA Current Source				
0x9A00	<0>	CURR_SOURCE_CONF	TURN_ON	Turn on current source: 0: 100µA turn off 1: 100µA turn on
	<7:1>			Reserved

15. Power On Reset (POR)

To ensure correct device initialization and operation of all macrocells in the device, the µASIC has a Power-On Reset (POR) circuit. The POR circuit achieves consistent behavior and predictable results during VDD power ramp up and power down. To accomplish this goal, the POR circuit releases a defined Power-Up sequence of internal events that initialize different macrocells inside the device.

15.1. POR General Operation

To start the Power-Up sequence, the voltage applied on the VDD should be higher than the POWER ON threshold (which can vary by PVT, but typical is 1.6 V). The operational V_{DD} range for the AM1U1514 is 1.71V…5.50V. Therefore, the Power-Up sequence will start earlier, as soon as the V_{DD} rises to the POWER ON threshold, but the VDD voltage itself must continue to ramp up to the operational voltage value. After the POR sequence has started, AM1U1514 will have a period of time to go through all the steps in the sequence and will be ready and completely operational after the Power-Up sequence is completed.

AM1U1514 is powered down and non-operational when the VDD voltage is between 0.6 V and -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher than the VDD voltage is applied to any other pin (although there is a 0.5 V margin due to forward drop voltage of the ESD protection diodes).

All pins are in HIGH IMPEDANCE state while the Power-Up sequence is taking place, and when the chip is powered down. The last step in the Power-Up sequence releases the IO structures from the HIGH IMPEDANCE state making the device operational. The design programmed into the chip defines the pin configuration of the device when operational. (The voltage on pins can't be higher than the VDD and this rule does apply to when the chip is powered on).

15.2. Power-Up Sequence

The Power-Up sequence of signals shown in Figure 15.1.

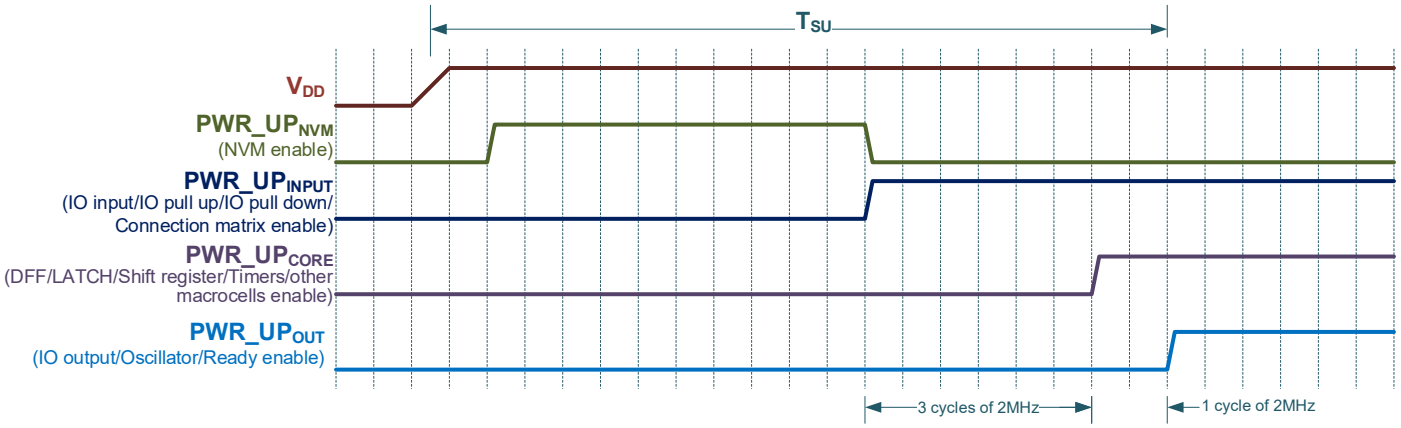


Figure 15.1. Power-Up sequence

As demonstrated by Figure 15.1 after the V_{DD} starts ramping up and crosses the POWER ON threshold, the on-chip NVM memory is enable. After that Input pins and Connection Matrix are enabled and all traces between all macrocells are routed. The macrocells like LUT, DFF, LATCH, Shift Register, Timers and others are initialized and stabilized for the next 3 cycles of 2MHz oscillator. After another one cycle READY signal and OSC outputs are enabled and outputs start to run. The output pins transition from HIGH IMPEDANCE to active at this point.

The completion time for the Power Up sequence varies by device type in the µASIC family. The completion time also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature to a degree that the times will even vary from chip to chip due to process influence.

15.3. Macrocells Output States During Power-Up Sequence

First, all macrocells have their output set to logic LOW, except the output pins which are in HIGH IMPEDANCE state, before the NVM is enabled. Then until the NVM is ready, all macrocell outputs states are unpredictable except the IOs. On the next step Input pins determined by external signals, LOGIC 1 is high, LOGIC 0 is low, LUTs and PDLY macrocell configured as edge detector work according to their inputs. All other macrocells are initialized in the next step. Lastly, READY signal, oscillator and the output pins become active as determined by the input signals. (Figure 15.2 describes the macrocell output signal states during the Power-Up sequence).

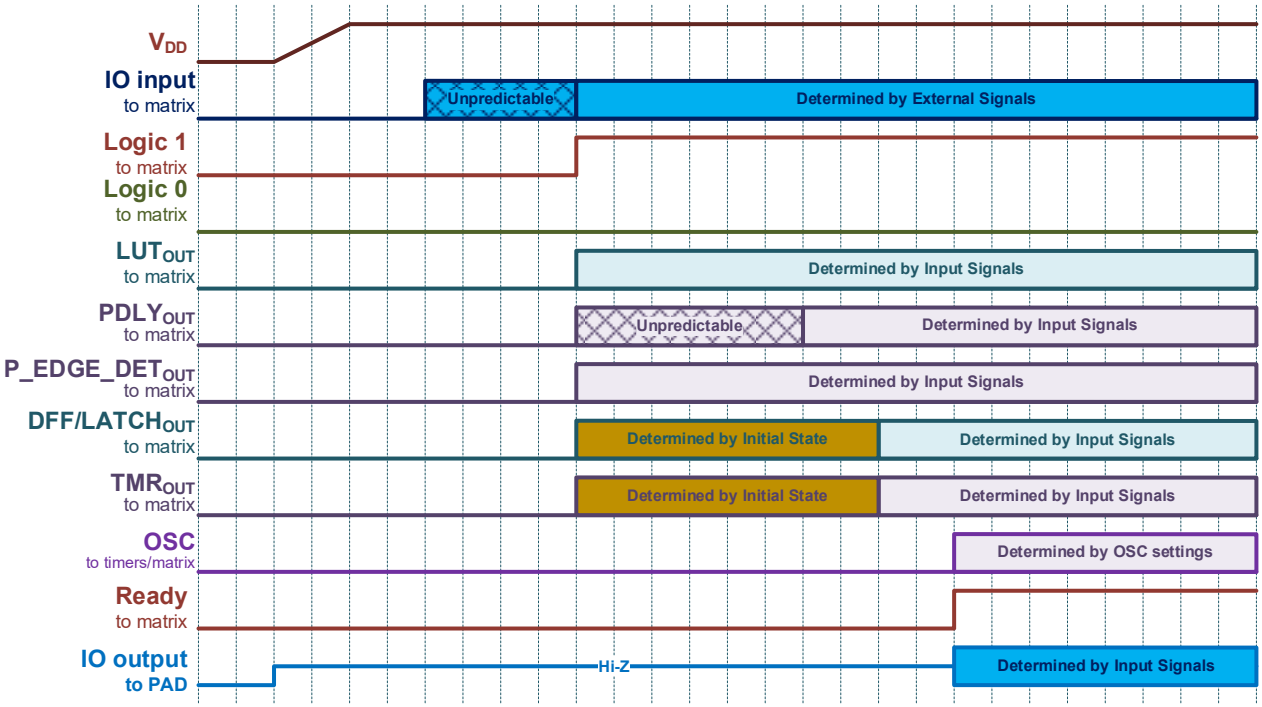


Figure 15.2. Internal Macrocell States during Power-Up sequence

15.4. Reset Events

To ensure the reliable operation of AM1U1514, multiple reset events have been anticipated:

- POR (Power-On Reset) also functions as a brownout reset – section 15.1;
- CRC-8 (Cyclic Redundancy Check 8) detects inadvertent alterations during the upload of programming code to the registers – section 9.1, Table 9.1;
- CRV (Continuous Registers Verification) involves continuously comparing dedicated register bits distributed throughout the memory with hardcoded values – section 9.2, Table 9.1.

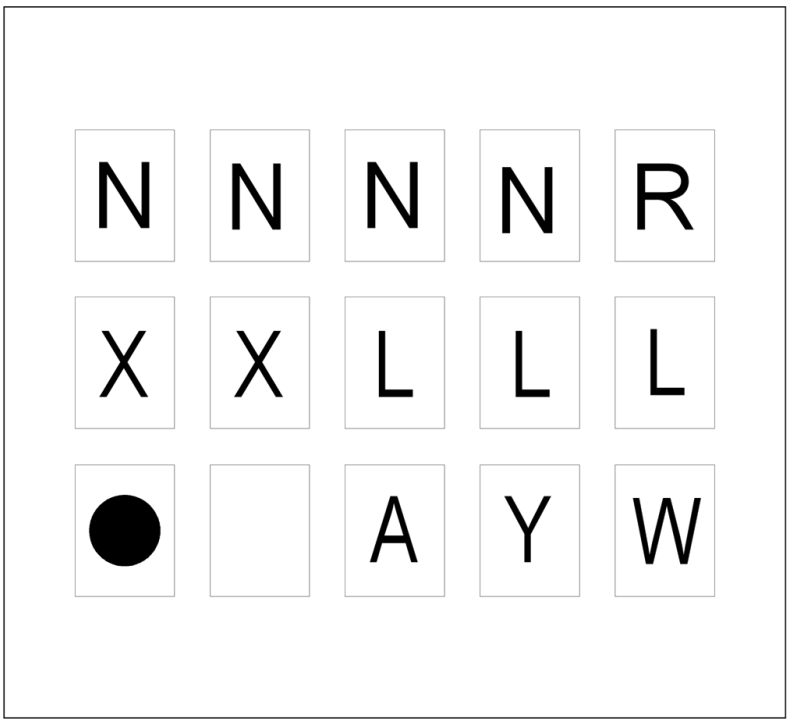
It should be noted that CRC-8 and CRV can be disabled by the corresponding registers SYS_SECURITY_CTRL_CRC_EN and SYS_SECURITY_CTRL_CRV_EN.

All reset events bring AM1U1514 into a predetermined state, enhancing the reliability of the entire system constructed with AM1U1514.

16. Abbreviations

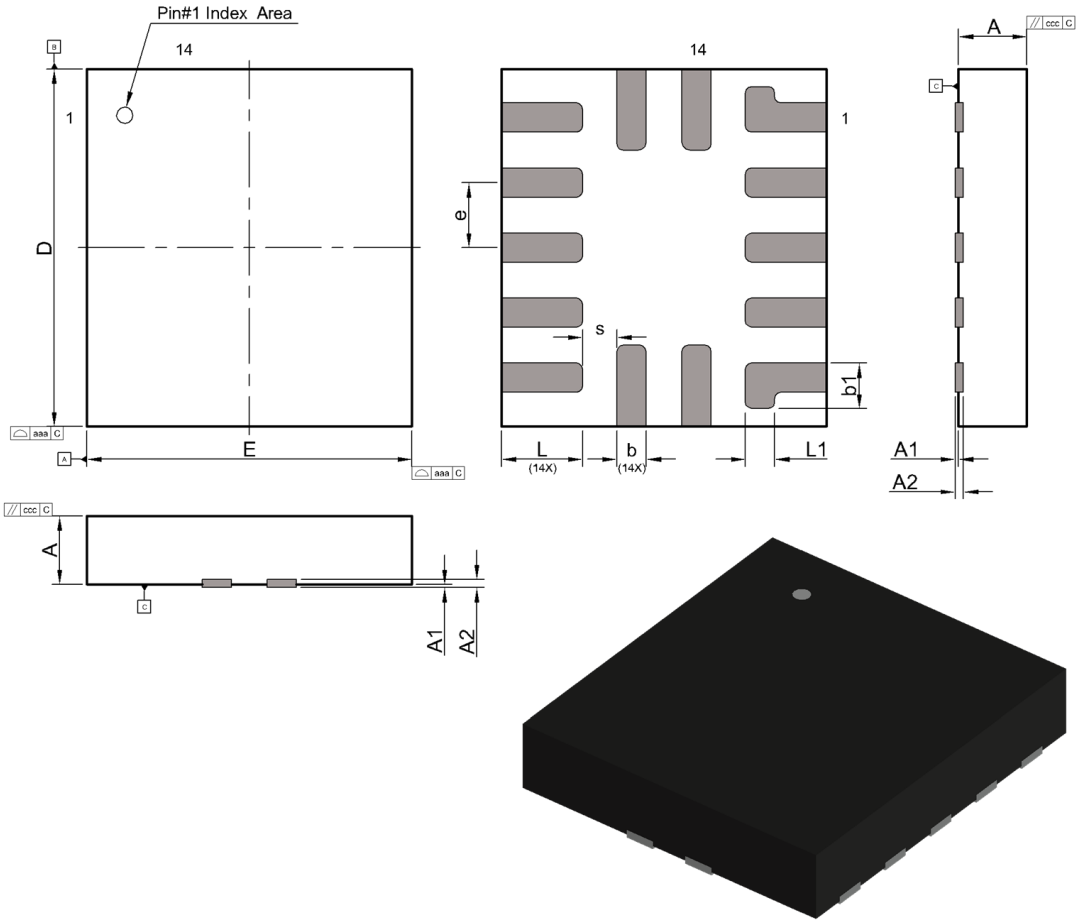
ACMP	Analog Comparator
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
CRC	Cyclic Redundancy Code
CRV	Continuous Registers Verification
CM	Connection Matrix
CMI	Connection Matrix Inputs
CMO	Connection Matrix Outputs
CV	Counted Value
DI	Digital Input
DIR	Direction
DILV	Digital Input Low Voltage
DIO	Digital Input/Output
ED	Edge Detector
EXTCLK	External Clock
IMC	Input Mode Control
IO	Input/Output
LV	Low Voltage
MF	Multi-Functional
N/A	Not Applicable
N/C	Not Connected
OD	Open Drain
OSC	Oscillator
OSG	One Shot Generator
PDLY	Programmable Delay
POR	Power On Reset
PP	Push Pull
PROP	Propagation
PW	Pulse Width
PWRDWN	Power Down
RA	Register Address
REG	Register
RST	Reset
SA	Slave Address
SHR	Shift Register
ST	Schmitt Trigger
TMR	Timer
TS	Temperature Sensor
VDD	Voltage Drain-Drain
VREF	Voltage Reference

17. Package Top Marking System Definition



N - Identification Code
R - Project Revision
X - Internal Code
L - Lot ID
A - Assembly site ID
Y - Assembly Year
W - Assembly Week

18. Package Drawing and Dimensions

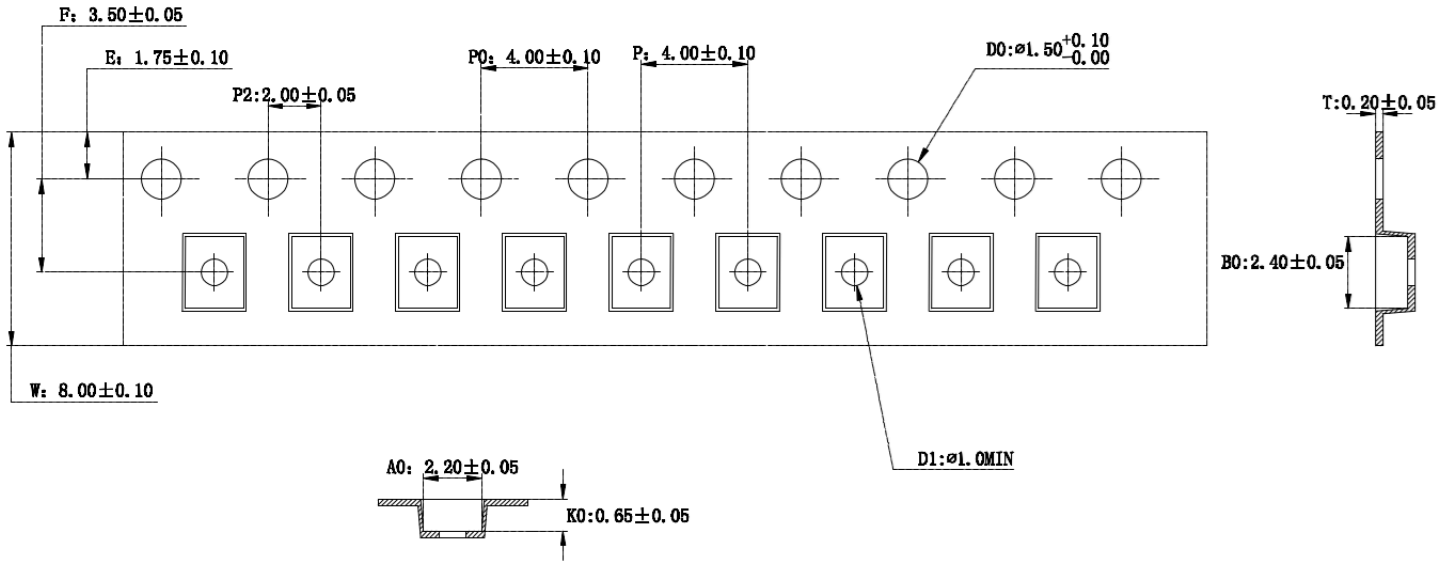


14-pin TQFN-A							
Dim	**Min**	**Max**	**Typ**	**Dim**	**Min**	**Max**	**Typ**
A	0.37	0.48	0.42	**D**	2.15	2.25	2.20
A1	-0.005	0.03	--	**E**	1.95	2.05	2.00
A2	0.017	0.10	0.03	**L**	0.45	0.55	0.50
b	0.13	0.23	0.18	**L1**	--	--	0.18
b1	--	--	0.28	**S**	--	--	0.21
e	--	--	0.40				
All Dimensions in mm							

19. Tape and Reel Specifications

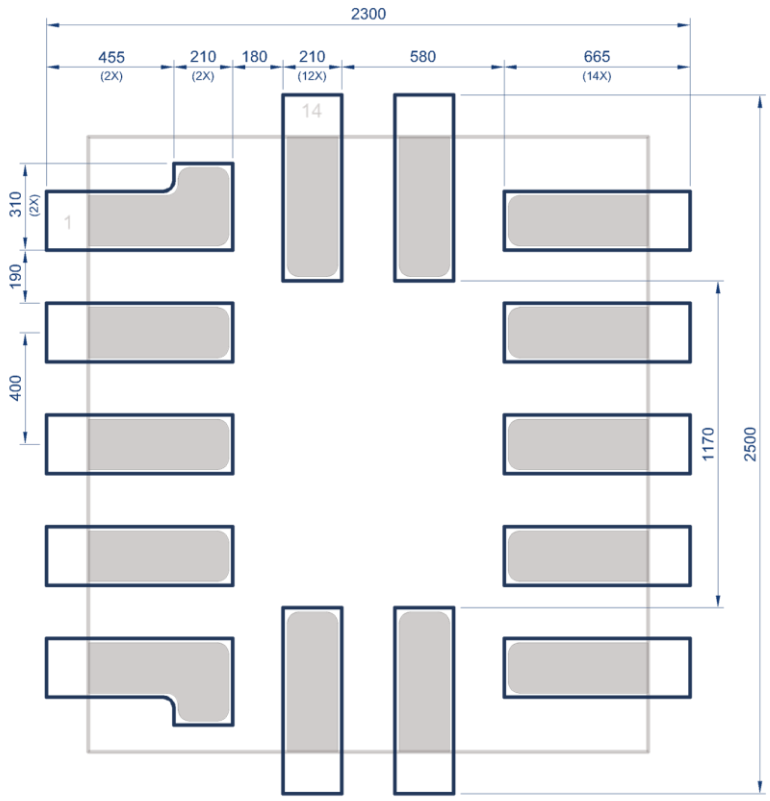
19.1. Carrier Tape Drawing and Dimensions

Package Type	W	E	F	P	P0	P2	D0	D1	A0	B0	K0	T	10P0
PMSFCQFN14 2.2X2.0X.425	8.00± 0.10	1.75± 0.10	3.50± 0.05	4.00± 0.10	4.00± 0.10	2.0± 0.05	1.50 +0.10 -0.00	Ø1.0 MIN	2.20± 0.05	2.40± 0.05	0.65± 0.05	0.20± 0.05	40.00 ±0.20



Note 19.1 All dimensions in millimeters unless otherwise stated.

20. Recommended Land Pattern



Unit: um

21. Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Weight: 0.0046 grams (Approximate)

22. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.85mm^3 (nominal). More information can be found at www.jedec.org.

23. Revision History

Date	Version	Change
January 13, 2025	Rev.001	Initial version
June 26, 2026	Rev.002	Updated characterization data. Added a section "Mechanical Data". Fixed typos.

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