AM1U1108

µASIC
Programmable Mixed-Signal IC

Description

The AM1U1108 is an ultra-small programmable µASIC featuring LUTs, Logic Macrocells, Timers, Oscillators, and more. Each Macrocell within the AM1U1108 contains multiple, configurable settings and initial states for maximum flexibility.

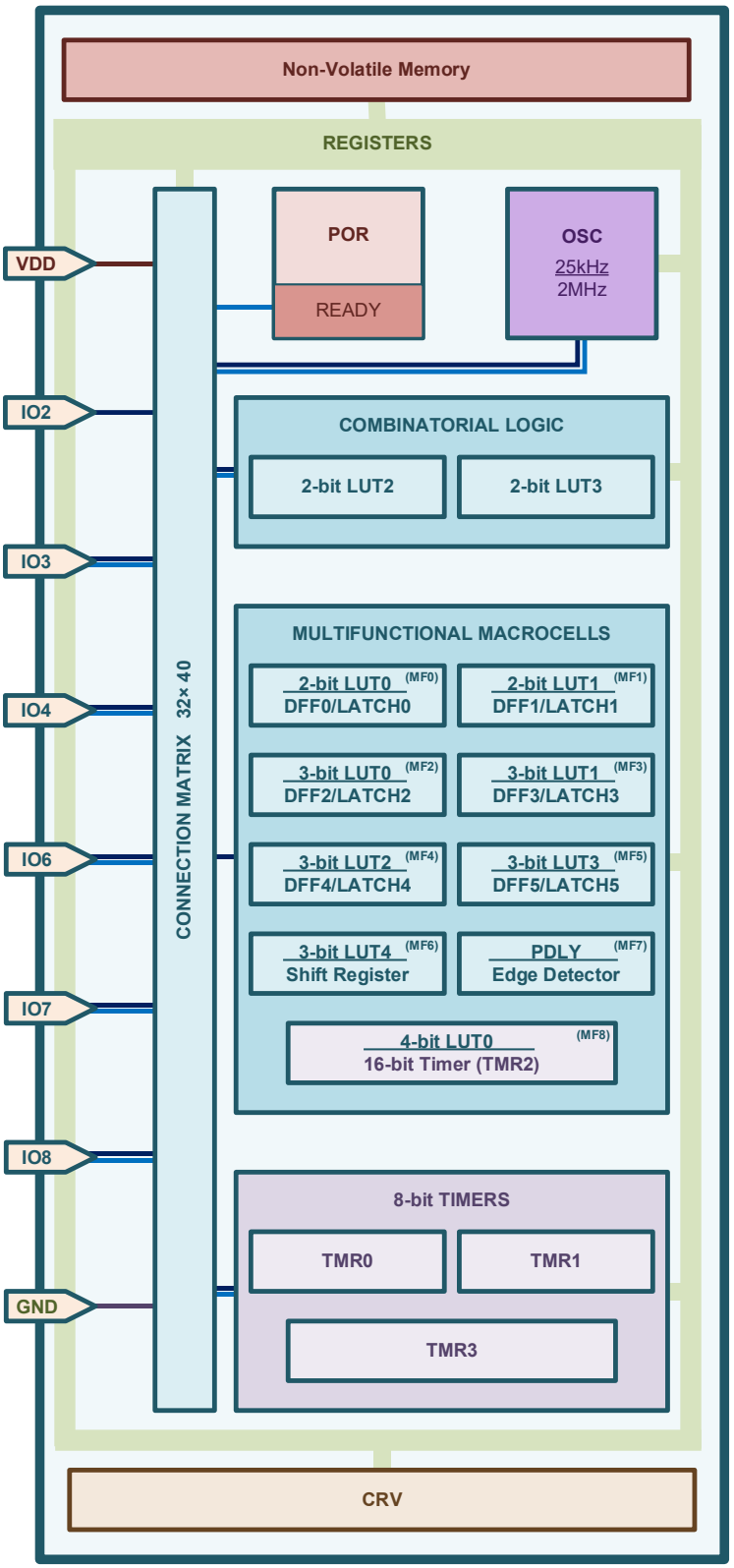
The AM1U1108 Macrocells are connected via hardware-defined matrix connections, not abstracted firmware. This enables asynchronous design at low power as well as more reliable operations compared to microcontrollers. Unlike a fixed ASIC, the timing and event sequences can be updated with a programming software change.

AM1U1108's functional reliability is enhanced by Continuous Register Verification (CRV).

Features

- 1.71 V to 5.50 V Supply
- Operating Temperature Range: -40°C to 85°C
- Six Digital Inputs/Outputs
  - One Digital Input
  - Five Digital Inputs/Outputs
- Two Combinatorial 2-bit Look Up Tables (LUTs)
- Nine Multifunctional Macrocell
  - Two Selectable D Flip-Flop (DFF)/Latches or 2-bit LUTs
  - Four Selectable D Flip-Flop/Latches or 3-bit LUTs
  - One Selectable Shift Register or 3-bit LUT
    - Shift Register (SR) – 16 stage/3 outputs
  - One Selectable 16-bit Timer with bidirectional counting (TMR) or 4-bit LUT
  - One Programmable Delay or Edge Detector
- Three 8-bit Timers with external clock/reset
- Oscillator (OSC)
- Power On Reset (POR)
- Data Protection Feature
  - Continuous Registers Verification (CRV)
- Package Options
  - 8-pin TQFN (1.0×1.2×0.42 mm, 0.4 mm pitch)

Architecture Block Diagram



The AM1U1108 (Figure 1, Table 1) has 6 multi-function IO pins which can function as a user-defined Input or Output. Refer to Table 1 for pin definitions.
All of the 6 user's defined IO pins on the AM1U1108, all pins can serve as both Digital Input and Digital Output, except IO2 which can only serving as a Digital Input PIN.

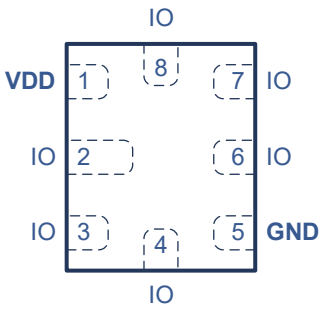


Figure 1. Top View (8-pin TQFN)

Table 1 Functional PIN Description

PIN # TQFN-8	PIN Name	Function	Input Options	Output Options
1	VDD	Power Supply	--	--
2	IO2	Digital Input	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	--
3	IO3	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
4	IO4	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
5	GND	Ground	--	--
6	IO6	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
7	IO7	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2
8	IO8	Digital IO	Digital Input w/o Schmitt Trigger Digital Input w/ Schmitt Trigger Digital Input Low Voltage	Push-Pull ×1 Push-Pull ×2 Open Drain NMOS ×1 Open Drain NMOS ×2 Open Drain PMOS ×1 Open Drain PMOS ×2

Macrocell Manifest

Macrocell Name	Description	Number of Units	Total Units	Referenced Section
IOs			**6**	**5**
Digital Input	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • 10 kΩ/100 kΩ/1 MΩ Pull-Down resistors	• One Digital Input	1	5.1, 5.3, 5.6.1, 5.4
Digital Input/Output	• Digital Input (low or normal voltage; with or without a Schmitt Trigger) • Open Drain Outputs: NMOS ×1(2), PMOS ×1(2) • Push Pull Outputs: PP ×1(2) • 10 kΩ/100 kΩ/1 MΩ Pull-Up/Pull-Down resistors	• Thirteen Digital IOs	5	5.1, 5.2, 5.3, 5.6.2, 5.6.3, 5.6.4, 5.6.5, 5.6.6, 5.5
Connection Matrix			**1**	**6**
Connection Matrix	• Digital matrix connections are based on user design	• Size 32×40	1	6.1, 6.2, 6.3
Combinatorial Logic Look Up Tables			**2**	**7**
2-bit LUT	• 2-bit Look-Up Table	• Two 2-bit LUTs	2	7.1
Multifunctional Macrocells			**9**	**8**
2-bit LUT	• 2-bit Look-Up Table	• Two 2-bit LUTs shared with DFF/LATCH w/o RST	2	8.1
3-bit LUT	• 3-bit Look-Up Table	• Four 3-bit LUTs shared with DFF/LATCH w/ RST • One 3-bit LUT shared with Shift Register	5	8.2, 8.3
4-bit LUT	• 4-bit Look-Up Table	• One 4-bit LUT shared with 16-bit Timer	1	8.4
DFF w/o RST	• D Flip-Flop w/o RST	• Two DFFs shared with 2-bit LUTs or LATCHs w/o RST	2	8.1
DFF w/ RST	• D Flip-Flop w/ RST	• Four DFFs shared with 3-bit LUTs or LATCHs w/ RST	4	8.2
LATCH w/o RST	• LATCH w/o RST	• Two LATCHs shared with 2-bit LUTs or DFFs w/o RST	2	8.1
LATCH w/ RST	• LATCH w/ RST	• Four LATCHs shared with 3-bit LUTs or DFFs w/ RST	4	8.2
Shift Register	• 16 stages/3 outputs • Two outputs with 1 to 16 selectable stages • One output with 1 stage	• One Shift Register shared with 3-bitLUT	1	8.3
16-bit TMR	• 16-bit Timer with bidirectional counting	• One 16-bit TMR shared with 4-bit LUT	1	8.5
PDLY	• Programmable Delay • 140 ns/280 ns/420 ns/560 ns @ VDD = 3.3 V	• One PDLY shared with Edge Detector	1	8.4
Edge Detector	• Rising Edge Detector • Falling Edge Detector • Both Edge Detector	• One Edge Detector shared PDLY	1	8.4
8-bit Timers			**3**	**9**

8-bit TMR	• One input from the Connection Matrix for DLY IN/RST IN
	• One input from the Connection Matrix for an external couter/clock source
	• Four Modes:
	  • Delay
	  • One Shot
	  • Frequency Detector
	  • Counter
		• Two 8-bit TMR with two inputs from Connection Matrix	2	9.1, 9.3

Macrocell Name	Description	Number of Units	Total Units	Referenced Section

8-bit TMR	• One input from the Connection Matrix which has a shared function of DLY IN or EXT CLK input
	• Four Modes:
	  • Delay
	  • One Shot
	  • Frequency Detector
	  • Counter
		• One 8-bit TMR with one input from Connection Matrix	1	9.4

Data Protection			**2**	**11**
CRV	• Continuous Registers Verification	•	1	11
Oscillators			**1**	**12**
25kHz 2MHz	• 25 kHz or 2 MHz selectable frequency or External clock source • $CLK_{Prescaler}$: /1, /2, /4, and /8 • Out clock frequency controlled with two outputs scaled by $OUT0_{Prescaler}$ and $OUT1_{Prescaler}$: /1, /2, /4, /8, /16, /32, /64 or /128	• One OSC (25kHz/2MHz)	1	12
POR			**2**	**13**
IO2 Reset	• Reset by events of IO2	•	1	13.4

Contents

1. Application Examples

The AM1U1108 is a programable mixed-signal IC which can be configured and used for a wide array of applications. Below you can find two simple use cases for the AM1U1108.

Example 1.1: Power sequencer (~40% of blocks are used)

Most of the complex electronic systems have definite power supply control to ensure that every part of the system starts up properly. This example (Figure 1.2) shows the implementation of such system based on AM1U1108. IN rising event runs the two-channel start up power supply sequence and IN falling event runs power down sequence (Figure 1.1).

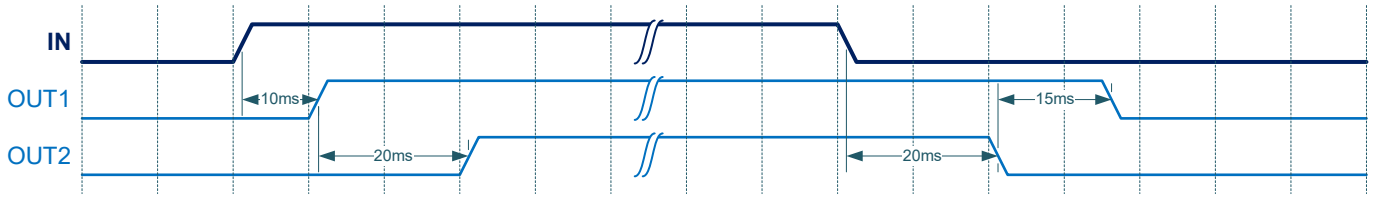


Figure 1.1. Power Sequencer requirements

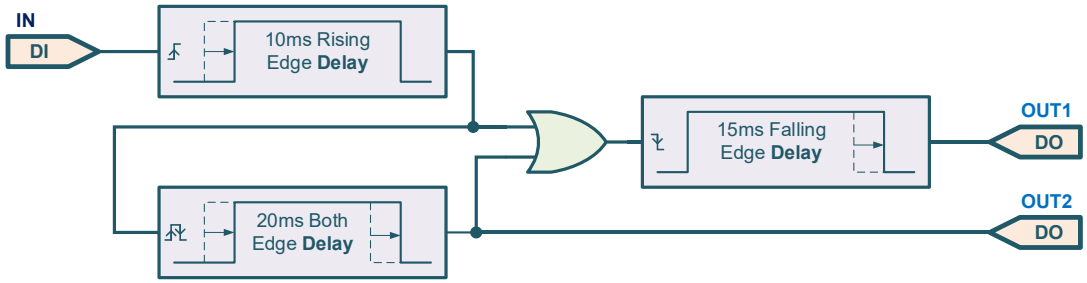


Figure 1.2. Power Sequencer implementation

Example 1.2 Watchdog timer (~35% of blocks are used)

AM1U1108 allows the customer to implement watchdog timer (Figure 1.4). If the device doesn't detect either rising or falling edge of IN signal during 100ms, it generates 500ms LOW pulse (Figure 1.3).

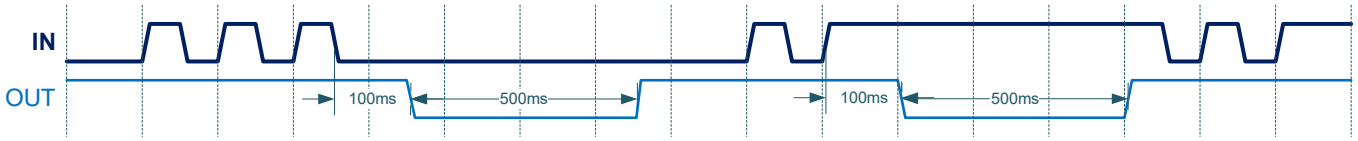


Figure 1.3. Watchdog requirements

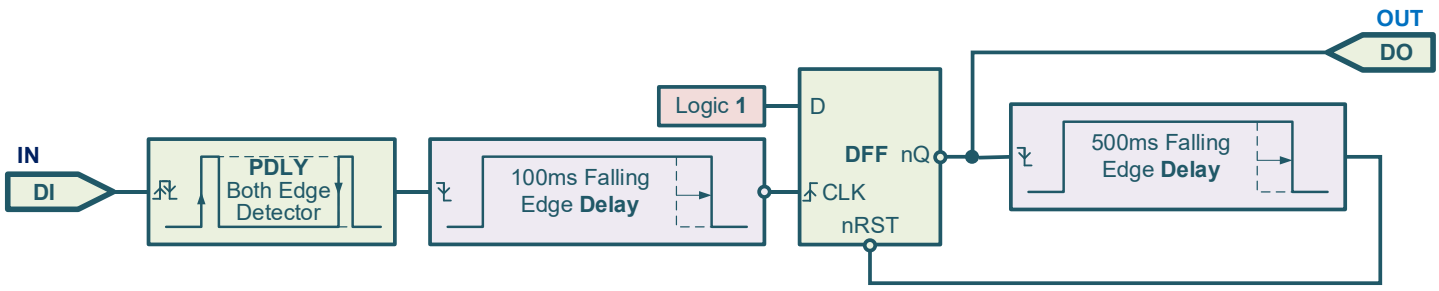


Figure 1.4. Watchdog implementation

2. How to Get Samples and Go to Production

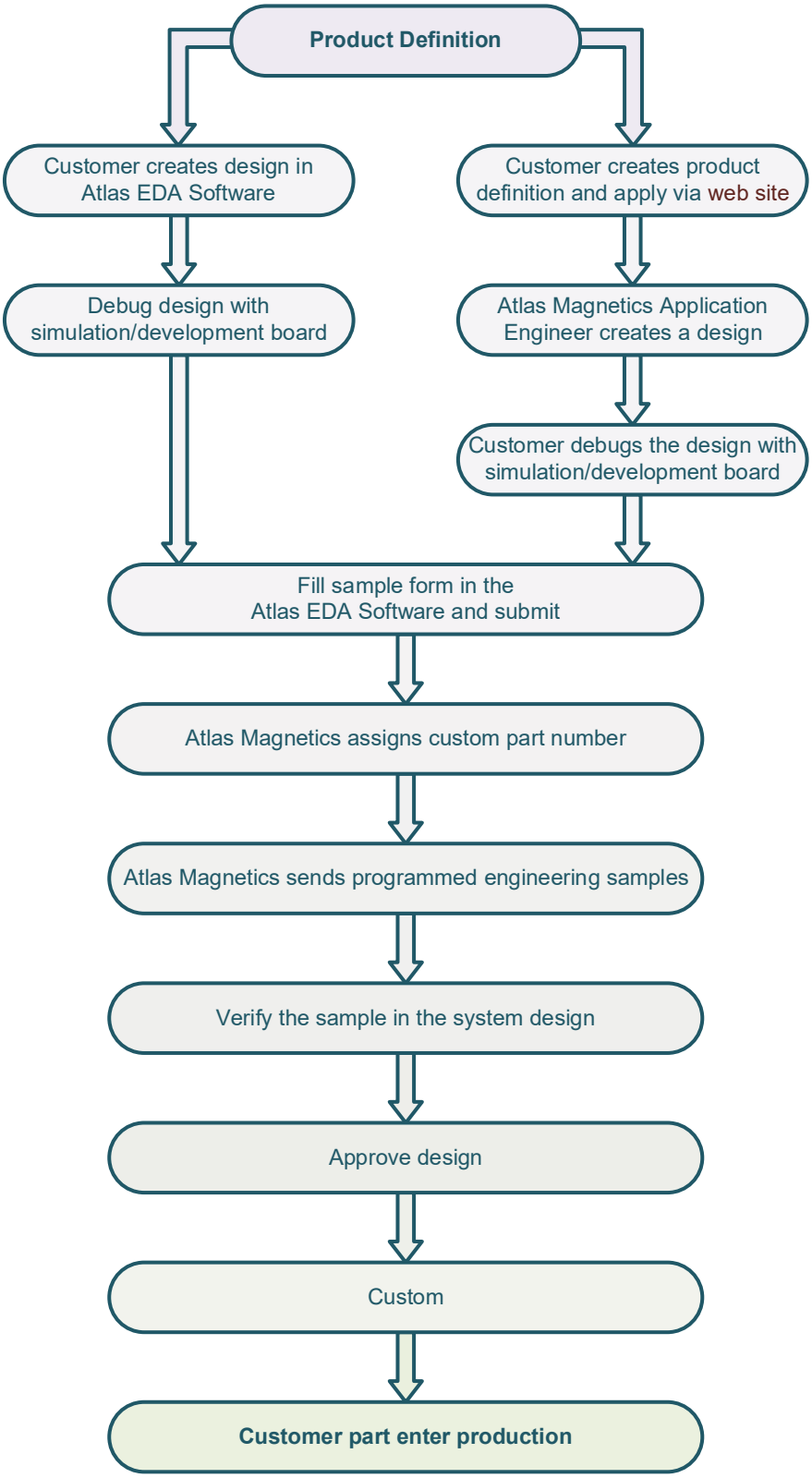


Figure 2.1. Steps to create a custom µASIC device

3. Ordering information

3.1. Ordering Information for Unprogrammed Part

Part Number	Type
AM1U1108	8-pin TQFN
AM1U1108 VTR	8-pin TQFN - Tape and Reel (3k units)

3.2. Ordering Information for Custom Programmed Part

Part Number	Type
xxxxxxxx	8-pin TQFN
xxxxxxxx	8-pin TQFN - Tape and Reel (3k units)

The custom program part number is created when design is submitted, get yours here (https://atlasmagnetics.com/contact).

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current Through VDD PIN (Per chip side, see Note 4.1)			100	mA
Maximum Average or DC Current Through GND PIN (Per chip side, see Note 4.1)			100	mA
Maximum Average or DC Current (Through pin)	PP×1	--	18	mA
	PP×2	--	28	mA
	OD(NMOS)×1	--	18	mA
	OD(NMOS)×2	--	28	mA
	OD(PMOS)×1		18	mA
	OD(PMOS)×2		28	mA
Current at Input PIN (Note 4.2)		-10.0	10.0	mA
Input leakage (Absolute Value)		--	2.0	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

Note 4.1 *The power rails are divided in two sides. PINs 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another*

Note 4.2 *Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings*

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.30	5.50	V
T_A	Operating Temperature		-40	25	85	°C
V_O	Operating Voltage Applied to any PIN in HIGH-Impedance State		GND – 0.3	--	V_{DD}+0.3	V
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF

4.3. General Specifications

Table 4.3. General characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.28	0.456	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.486	1.6	1.652	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off theChip	1.348	1.5	1.541	V

4.4. IO Specifications

Table 4.4. IO Electrical Characteristics

@ V_{DD} = 1.71V to 5.50V, T = - 40 °C to +85 °C Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{IH}	HIGH-Level Input Voltage	Digital input w/o Schmitt trigger (Note 4.3)	0.7xV_{DD}	--	V_{DD}+0.3	V
		Digital input w/ Schmitt trigger	0.8xV_{DD}	--	V_{DD}+0.3	V
		Digital input low voltage (Note 4.3)	1.05	--	V_{DD}+0.3	V
V_{IL}	LOW-Level Input Voltage	Digita input w/o Schmitt trigger (Note 4.3)	GND-0.3	--	0.3xV_{DD}	V
		Digital input w/ Schmitt trigger	GND-0.3	--	0.2xV_{DD}	V
		Digital input low voltage (Note 4.3)	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Digital input w/ Schmitt trigger	--	0.5	--	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -100 µA, V_{DD} = 1.8 V	1.793	1.795	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -100 µA, V_{DD} = 1.8 V	1.796	1.797	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -3 mA, V_{DD} = 3.3 V	3.200	3.219	-	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -3 mA, V_{DD} = 3.3 V	3.250	3.259	--	V
		Push-Pull ×1, Open Drain PMOS ×1, I_{OH} = -5 mA, V_{DD} = 5.0 V	4.880	4.902	--	V
		Push-Pull ×2, Open Drain PMOS ×2, I_{OH} = -5 mA, V_{DD} = 5.0 V	4.939	4.950	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.0026	0.0034	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 100 µA, V_{DD} = 1.8 V	--	0.0012	0.0017	V
		Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.0442	0.0554	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	0.0223	0.0281	V
		Push-Pull ×1, Open Drain NMOS ×1, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	0.0542	0.0693	V
		Push-Pull ×2, Open Drain NMOS ×2, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	0.0275	0.0354	V
I_{OH}	HIGH-Level Output Current (see Note 4.4)	Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = VDD - 0.2, V_{DD} = 1.8 V	-2.622	-3.252	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = VDD - 0.2, V_{DD} = 1.8 V	-5.123	-6.463	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4 V, V_{DD} = 3.3 V	-20.341	-24.741	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4 V, V_{DD} = 3.3 V	-36.466	-46.501	--	mA
		Push-Pull ×1, Open Drain PMOS ×1, V_{OH} = 2.4 V, V_{DD} = 5.0 V	-58.441	-67.107	--	mA
		Push-Pull ×2, Open Drain PMOS ×2, V_{OH} = 2.4 V, V_{DD} = 5.0 V	-105.513	-124.048	--	mA
I_{OL}	LOW-Level Output Current (see Note 4.3)	Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.15 V, V_{DD} = 1.8 V	3.794	4.631	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.15 V, V_{DD} = 1.8 V	7.463	9.100	--	mA
		Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.4 V, V_{DD} = 3.3 V	19.191	24.155	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.4 V, V_{DD} = 3.3 V	37.496	47.278	--	mA
		Push-Pull ×1, Open Drain NMOS ×1, V_{OL} = 0.4 V, V_{DD} = 5.0 V	26.735	34.613	--	mA
		Push-Pull ×2, Open Drain NMOS ×2, V_{OL} = 0.4 V, V_{DD} = 5.0 V	51.917	67.477	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
R_{PULL}	Pull-Up or Pull-Down Resistance	1000 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	910.732	1000	1161.136	kΩ
		100 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	94.058	100	116.915	kΩ
		10 kΩ; For Pull-Up V_{IN} = GND; For Pull-Down V_{IN} = V_{DD}	9.154	10	12.294	kΩ
C_{IN}	Input Capacitance		--	4	--	pF
Note 4.3	*No hysteresis*					
Note 4.4	*DC or average current through any pin should not exceed value given in Absolute Maximum Conditions*					

4.5. Typical Current Consumption

Table 4.5. Typical Current Estimated for Each Macrocell

Symbol	Parameter	Note	VDD = 1.8 V	VDD = 3.3 V	VDD = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent	0.349	0.377	0.414	µA
		OSC 2 MHz, OFF State	--	--	<1	nA
		OSC 2 MHz, IDLE State	174.2	174.2	174.2	nA
		OSC 2 MHz, PreScaler = 1	9.542	20.719	38.265	µA
		OSC 2 MHz, PreScaler = 2	8.823	19.321	35.932	µA
		OSC 2 MHz, PreScaler = 4	8.493	18.684	34.874	µA
		OSC 2 MHz, PreScaler = 8	8.296	18.304	34.239	µA
		OSC 25 kHz, OFF State	--	--	<1	nA
		OSC 25 kHz, IDLE State	43	42	41	nA
		OSC 25 kHz, PreScaler = 1	0.175	0.271	0.303	µA
		OSC 25 kHz, PreScaler = 2	0.167	0.253	0.372	µA
		OSC 25 kHz, PreScaler = 4	0.162	0.245	0.358	µA
		OSC 25 kHz, PreScaler = 8	0.160	0.240	0.350	µA

4.6. Timing Estimator

Table 4.6 Typical Propagation Time (t_{PROP}) for Each Macrocell

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		VDD = 5.0 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
DI w/o ST	DO PP×1	IO	45.8	29.8	14.2	10.6	8.8	7.0	ns
DI w/o ST	DO PP×2	IO	45.1	29.2	14.1	10.4	8.7	6.9	ns
DI w/ ST	DO PP×1	IO	47.3	31.5	15.1	11.4	9.6	7.5	ns
DI w/ ST	DO PP×2	IO	47.1	31.2	14.8	11.2	9.4	7.4	
DI LV	DO PP×1	IO	27.7	55.9	9.1	21.7	4.5	15.4	ns
DI LV	DO PP×2	IO	27.1	54.9	9.3	21.5	5.4	15.3	ns
DI w/o ST	DO NMOS×1	IO	--	28.5	--	10.0	--	6.8	ns
DI w/o ST	DO NMOS×2	IO	--	28	--	9.9	--	6.7	ns
DI w/o ST	DO PMOS×1	IO	43.1	--	13.4	--	8.3	--	ns
DI w/o ST	DO PMOS×2	IO	42.8	--	13.2	--	8.1	--	ns
IN	OUT	2-bit LUT	16.3	17.4	5. 6	6.4	4.9	4.7	ns
IN	OUT	3-bit LUT	19.12	22.3	6.7	7.8	5.8	5.7	ns
IN	OUT0	3-bit LUT	19.1	22.9	6.9	8.1	6.0	5.9	ns
IN	OUT1	3-bit LUT	18.8	22.1	6.5	7.7	5.8	5.6	ns
IN	OUT	4-bit LUT	21.4	22.5	7.3	8.0	6.1	5.8	ns
CLK	Q	DFF w/o nRST(nSET)	22.3	16.5	7.4	6.7	5.1	4.7	ns
CLK	nQ	DFF w/o nRST(nSET)	20.1	15.5	6.9	6.2	4.6	4.3	ns
CLK	Q	DFF w/ nRST(nSET)	23.0	17.4	7.7	7.0	5.1	4.9	ns
nRST	Q	DFF w/ nRST	--	22.5	--	7.6	--	5.0	ns
nSET	Q	DFF w/ nSET	29.9	--	9.9	--	5.9	--	ns
CLK	nQ	DFF w/ nRST(nSET)	21.3	17.4	7.4	6.8	4.9	4.7	ns
nRST	nQ	DFF w/ nRST	26.4	--	8.6	--	5.2	--	ns
nSET	nQ	DFF w/ nSET	--	24.0	--	8.0	--	5.3	ns

Start Point	End point	Note	VDD = 1.8 V		VDD = 3.3 V		VDD = 5.0 V		Unit
			Low to High	High to Low	Low to High	High to Low	Low to High	High to Low	
D	Q	LATCH w/o nRST(nSET)	21.6	21.9	7.3	7.1	4.8	4.9	ns
nL	Q	LATCH w/o nRST(nSET)	24.7	19.1	8.1	9.0	5.5	5.6	ns
D	nQ	LATCH w/o nRST(nSET)	24.1	15.0	7.7	5.8	4.9	5.3	ns
nL	nQ	LATCH w/o nRST(nSET)	22.4	17.4	7.5	7.5	5.0	4.9	ns
D	Q	LATCH w/ nRST(nSET)	21.7	22.3	7.4	7.5	4.8	4.8	ns
nL	Q	LATCH w/ nRST(nSET)	24.9	19.1	8.1	7.6	5.3	5.3	ns
nRST	Q	LATCH w/ nRST	21.4	21.9	7.4	7.4	4.9	4.9	ns
nSET	Q	LATCH w/ nSET	29.9	17.6	9.8	7.3	5.8	5.1	ns
D	nQ	LATCH w/ nRST(nSET)	26.2	15.9	8.4	6.3	5.1	4.3	ns
nL	nQ	LATCH w/ nRST(nSET)	22.5	18.5	7.6	7.4	5.0	5.1	ns
nRST	nQ	LATCH w/ nRST	25.9	17.9	8.0	6.7	5.1	4.6	ns
nSET	nQ	LATCH w/ nSET	21.8	23.8	7.5	7.9	4.9	5.2	ns
CLK	OUT0	Shift register	25.5	24.2	8.6	9.2	5.7	6.4	ns
CLK	OUT1	Shift register	28.1	25.6	9.0	9.5	6.0	6.8	ns
CLK	Q[1]	Shift register	25.8	19.7	8.3	8.0	5.5	5.6	ns
CLK	nOUT1	Shift register	30.3	23.3	9.7	9.0	6.4	6.4	ns
nRST	OUT0	Shift register	--	27.3	--	9.1	--	6.2	ns
nRST	OUT1	Shift register	--	28.1	--	9.6	--	6.5	ns
nRST	Q[1]	Shift register	--	22.7	--	7.9	--	5.3	ns
nRST	nOUT1	Shift register	33.3	--	11.1	--	7.1	--	ns
IN	OUT	8-bit TMR (Delay)	32.3	35.0	11.0	12.0	7.3	7.0	ns
IN	OUT	8-bit TMR (One-Shot)	39.3	--	13.0	--	8.2	--	ns
RST	OUT	8-bit TMR (Counter)	51.8	--	16.8	--	10.8	--	ns
IN	OUT	8-bit TMR (Frequency Detector)	38.3	--	12.7	--	8.2	--	ns
IN	OUT	8-bit TMR (Edge Detector)	28.8	--	9.7	--	5.8	--	ns
CLK	OUT	8-bit TMR (Delay)	63.5	60.5	21.0	20.5	13.0	13.0	ns
CLK	OUT	8-bit TMR (One-Shot)	--	60.5	--	20.5	--	13.0	ns
CLK	OUT	8-bit TMR (Counter)	60.5	60.5	20.0	20.5	12.0	13.0	ns
CLK	OUT	8-bit TMR (Frequency Detector)	--	60.5	--	20.5	--	13.0	ns
IN	OUT	8-bit TMR (Delayed Edge Detector)	72.5	--	24.0	--	15.0	--	
IN	OUT	16-bit TMR (Delay)	33.0	30.0	12.0	10.0	8.0	5.0	ns
IN	OUT	16-bit TMR (One-Shot)	40.0	--	13.5	--	8.5	--	ns
RST	OUT	16-bit TMR (Counter)	55.5	--	18.5	--	12.5	--	ns
IN	OUT	16-bit TMR (Frequency Detector)	39.0	--	13.0	--	8.5	--	ns
CLK	OUT	16-bit TMR (Delay)	106.0	102.0	34.0	34.0	21.0	21.0	ns
CLK	OUT	16-bit TMR (One-Shot)	--	101.0	--	33.0	--	21.0	ns
CLK	OUT	16-bit TMR (Counter)	106.0	75.0	35.0	25.0	22.0	16.0	ns
CLK	OUT	16-bit TMR (Frequency Detector)	--	101.0	--	33.0	--	21.0	ns

Table 4.7 Expected Delays and Widths for Programmable Delay/Edge Detector

Symbol	Parameter	Note	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
T_{Width}	Width, 140ns	Mode:(any)Edge Detect, Edge Detect Output	123.7	118.8	117.2	ns
T_{Width}	Width, 280ns	Mode:(any)Edge Detect, Edge Detect Output	256.7	254.4	254.8	ns
T_{Width}	Width, 420ns	Mode:(any)Edge Detect, Edge Detect Output	388.6	387.7	390.3	ns
T_{Width}	Width, 560ns	Mode:(any)Edge Detect, Edge Detect Output	521.2	522.0	526.8	ns
T_{PROP}	Delay, 140ns	Mode:(any)Edge Detect, Edge Detect Output	34.6	11.1	7.3	ns
T_{PROP}	Delay, 280ns	Mode:(any)Edge Detect, Edge Detect Output	34.6	11.2	7.3	ns
T_{PROP}	Delay, 420ns	Mode:(any)Edge Detect, Edge Detect Output	34.5	11.2	7.3	ns
T_{PROP}	Delay, 560ns	Mode:(any)Edge Detect, Edge Detect Output	34.6	11.2	7.3	ns
T_{DLY}	Delay, 140ns	Mode: Both Edge Delay, Edge Detect Output	158.2	130.0	124.5	ns
T_{DLY}	Delay, 280ns	Mode: Both Edge Delay, Edge Detect Output	291.3	265.6	262.2	ns
T_{DLY}	Delay, 420ns	Mode: Both Edge Delay, Edge Detect Output	423.1	398.8	397.6	ns
T_{DLY}	Delay, 560ns	Mode: Both Edge Delay, Edge Detect Output	555.9	533.2	534.1	ns

4.7. OSC Specifications

4.7.1. 25 kHz Oscillator

Table 4.8 25 kHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min, kHz	Max, kHz	Min, kHz	Max, kHz	Min, kHz	Max, kHz
1.8 V ±5%	24.740	25.240	22.217	25.249	22.217	28.870
3.3 V ±10%	24.713	25.264	22.237	25.264	23.237	28.905
5 V ±10%	24.708	25.540	22.278	25.278	22.229	29.272
2.5 V…4.5 V	24.708	25.314	22.230	25.315	22.230	28.951
1.71 V…5.50 V	24.708	25.726	22.217	25.726	22.217	29.368

Table 4.9 25 kHz OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max	Min	Max
1.8 V ±5%	-1.04%	0.96%	-11.13%	1.00%	-11.13%	15.48%
3.3 V ±10%	-1.15%	1.06%	-11.05%	1.06%	-7.05%	15.62%
5 V ±10%	-1.17%	2.16%	-10.89%	1.11%	-11.08%	17.09%
2.5 V…4.5 V	-1.17%	1.26%	-11.08%	1.26%	-11.08%	15.80%
1.71 V…5.50 V	-1.17%	2.90%	-11.13%	2.90%	-11.13%	17.47%

Table 4.10 25 kHz OSC Power on time at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.71	361.8	483.2	20.01	40.42
1.80	360.5	486.8	20.01	40.44
3.30	345.8	472.7	20.01	40.47
5.00	324.7	424.3	20.01	40.48
5.50	320.6	425.2	20.01	40.41

Table 4.11 25 kHz OSC Frequency Settling Time

Parameter	Description	Normal	Fast	Unit
Frequency Settling Time	To reach the 2.5% error	1	1	Cycles

Note 4.5 The OSC frequency error during settling time is less than 10%

4.7.2. 2 MHz Oscillator

Table 4.12 2 MHz OSC Frequency Limits

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min, MHz	Max, MHz	Min, MHz	Max, MHz	Min, MHz	Max, MHz
1.8 V ±5%	1.976	2.024	1.838	2.074	1.780	2.260
3.3 V ±10%	1.967	2.029	1.827	2.074	1.789	2.258
5 V ±10%	1.964	2.047	1.822	2.093	1.792	2.270
2.5 V…4.5 V	1.961	2.042	1.822	2.086	1.789	2.271
1.71 V…5.50 V	1.961	2.060	1.822	2.105	1.780	2.292

Table 4.13 2 MHz OSC Frequency Error (Error Calculated in Relation to Nominal Value)

Power Supply Range V_{DD}, V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min	Max	Min	Max	Min	Max
1.8 V ±5%	-1.20%	1.20%	-8.10%	3.70%	-11.00%	13.00%
3.3 V ±10%	-1.65%	1.45%	-8.65%	3.70%	-10.55%	12.90%
5 V ±10%	-1.80%	2.35%	-8.90%	4.65%	-10.40%	13.50%
2.5 V…4.5 V	-1.95%	2.10%	-8.90%	4.30%	-10.55%	13.55%
1.71 V…5.50 V	-1.95%	3.00%	-8.90%	5.25%	-11.00%	14.60%

Table 4.14 2 MHz OSC Power on time at Room Temperature

Power Supply Range V_{DD}, V	Normal		Fast	
	Typ, us	Max, us	Typ, us	Max, us
1.71	77.27	96.84	0.500	0.506
1.80	76.83	96.72	0.500	0.507
3.30	71.28	89.14	0.500	0.508
5.00	64.48	80.60	0.501	0.509
5.50	61.04	75.95	0.501	0.508

Table 4.15 2 MHz OSC Frequency Settling Time

Parameter	Description	Normal	Fast	Unit
Frequency Settling Time	To reach the 2.5% error	7	10	Cycles

Note 4.6 The OSC frequency error during settling time is less than 10%

5. IO PINs

5.1. Input Modes

Each of the IOs can be configured as a Digital Input with or without a buffered Schmitt trigger or they can also be configured as a Digital Input Low Voltage.

5.2. Output Modes

All IOs except IO2 can be configurable as digital outputs.

5.3. Pull Up/Down Resistors

All IOs have an option for user selectable resistors connected to the input structure, with the selectable values being 10 kΩ, 100 kΩ and 1 MΩ. In the case of IO2, the resistors are fixed to a pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as pull-up or pull-downs.

5.4. IO Structure (for IO2)

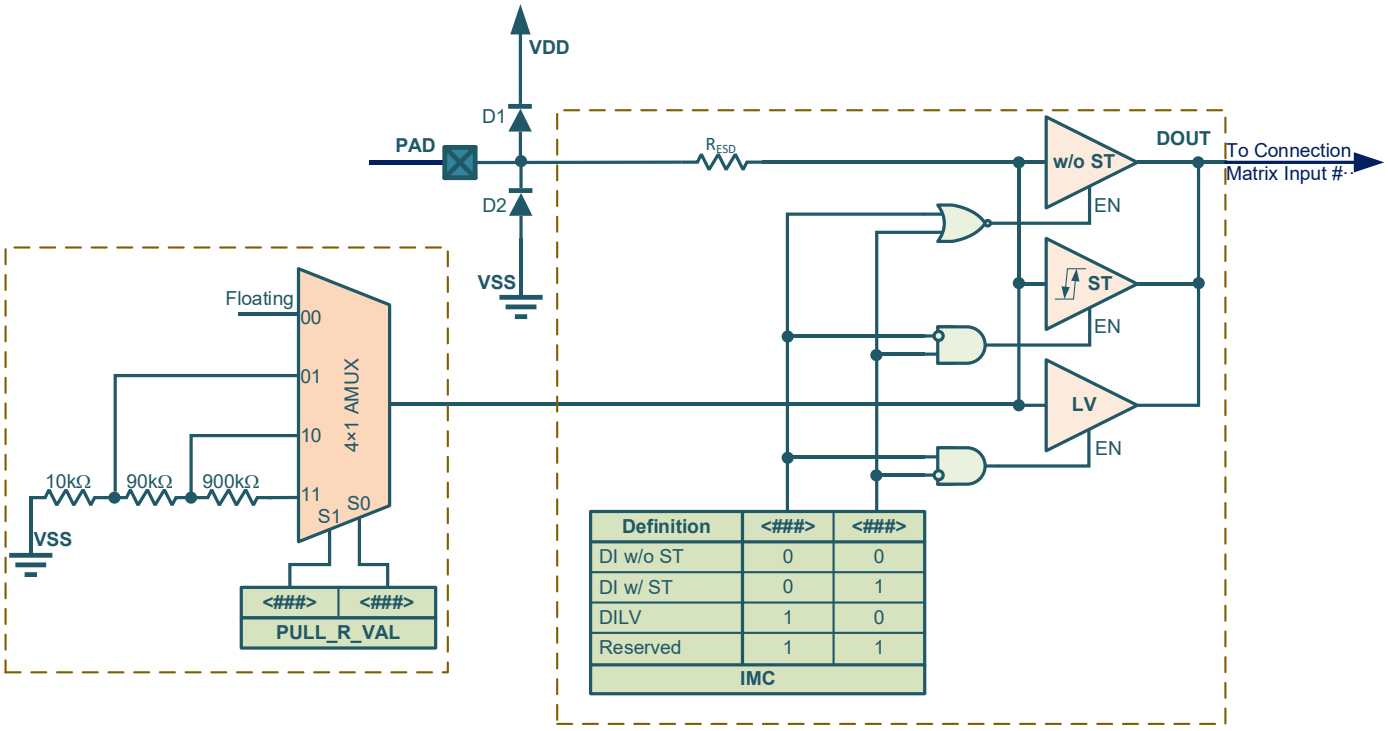


Figure 5.1. IO2 Structure Diagram

5.5. IO Structure (for IO3, IO4, IO6, IO7, IO8)

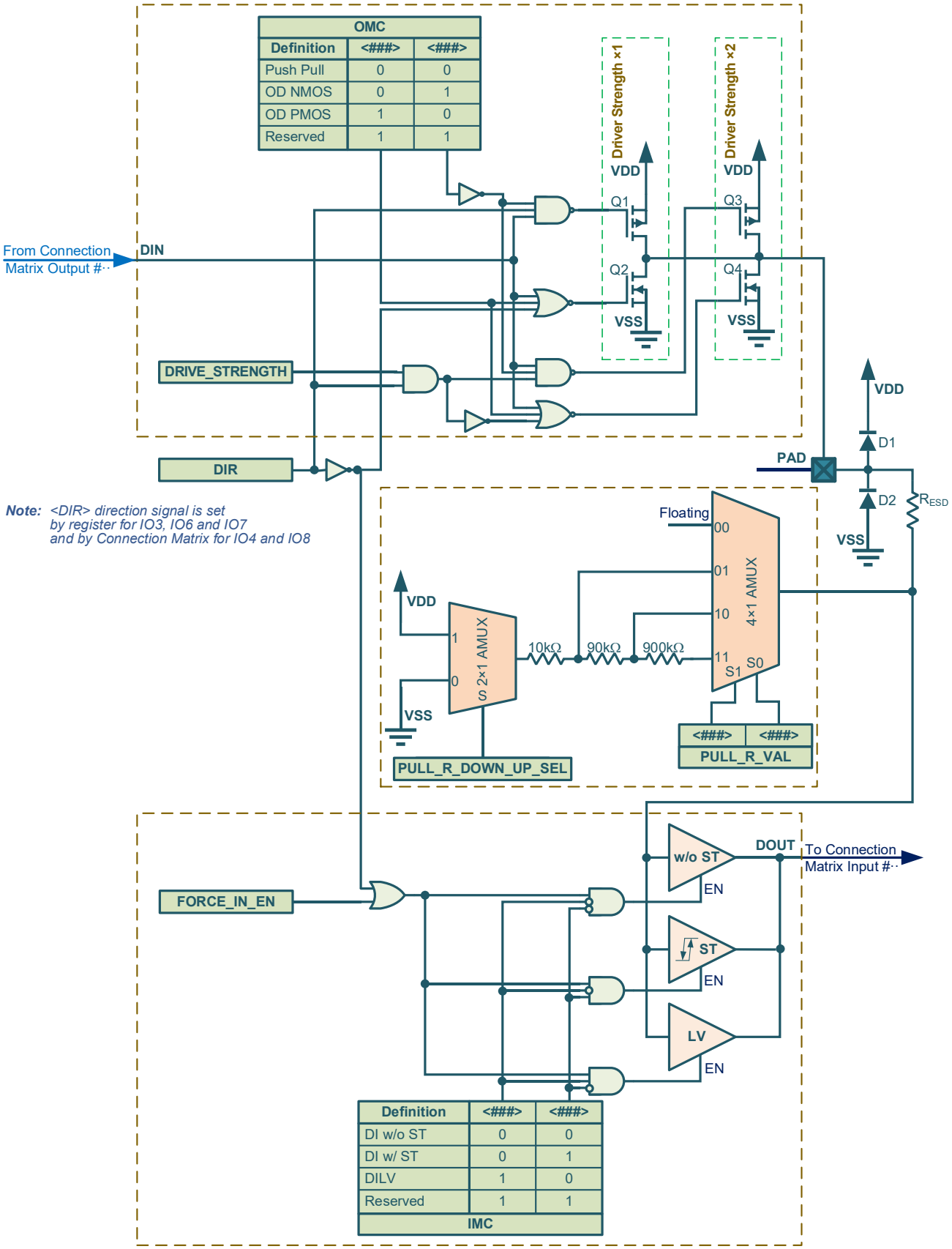


Figure 5.2. IO Structure Diagram

5.6. IO Register Settings

5.6.1. IO2 Register Settings

Table 5.1 IO2 Register Settings

Register Bit Address	Register Name	Register Definition
IO2		
<408:407>	IO2_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<410:409>	IO2_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.6.2. IO3 Register Settings

Table 5.2 IO3 Register Settings

Register Bit Address	Register Name	Register Definition
IO3		
<404>	IO3_DIR	Direction: 0: Input 1: Output
<369>	IO3_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<413:412>	IO3_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<415:414>	IO3_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<337>	IO3_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<418>	IO3_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<417:416>	IO3_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.6.3. IO4 Register Settings

Table 5.3 IO4 Register Settings

Register Bit Address	Register Name	Register Definition
IO4		
<370>	IO4_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<420:419>	IO4_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<422:421>	IO4_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<338>	IO4_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<425>	IO4_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<424:423>	IO4_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.6.4. IO6 Register Settings

Table 5.4 IO6 Register Settings

Register Bit Address	Register Name	Register Definition
IO6		
<405>	IO6_DIR	Direction: 0: Input 1: Output
<371>	IO6_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<427:426>	IO6_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<429:428>	IO6_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<339>	IO6_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<432>	IO6_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<431:430>	IO6_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.6.5. IO7 Register Settings

Table 5.5 IO7 Register Settings

Register Bit Address	Register Name	Register Definition
IO7		
<406>	IO7_DIR	Direction: 0: Input 1: Output
<372>	IO7_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<434:433>	IO7_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<436:435>	IO7_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<340>	IO7_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<439>	IO7_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<438:437>	IO7_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

5.6.6. IO8 Register Settings

Table 5.6 IO8 Register Settings

Register Bit Address	Register Name	Register Definition
IO8		
<373>	IO8_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<441:440>	IO8_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<443:442>	IO8_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<341>	IO8_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<446>	IO8_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
<445:444>	IO8_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

6. Connection Matrix

The AM1U1108 Connection Matrix is used to create internal routing between cells what in turn allows to get customized functionality of the device. All of the connections of each cell within the AM1U1108 are defined by the value of corresponding register bits, which values is loaded from NVM during power up of the device.

The Connection Matrix has 32 inputs and 40 outputs. Each individual input to the Connection Matrix is hard-wired to a particular macrocell output: including IOs, Multifunctional Macrocells, Logic **1**, Logic **0,** etc. Each individual output from the Connection Matrix is hard-wired to a particular macrocell input and uses a 5-bit register to select one of the 32 input lines (see Section 6.1 Example of Matrix Connection).

For a complete list of the AM1U1108 register table, see Section 15 Appendix A – AM1U1108 Register Definition.

6.1. Example of Matrix Connection

A simple design example to showcase the Matrix Connection is shown in the Figure 6.1.

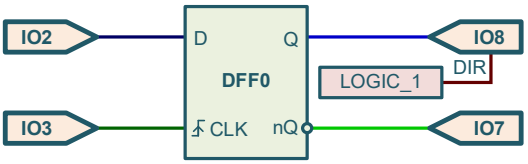


Figure 6.1. Example Design

Figure 6.2 and Figure 6.3 explain the strategy of Matrix Connection configuration.

Function	IN	Logic 0	IO2	IO3	IO4	DFF0 (Q)	DFF1 (Q)	. . .	. . .	. . .	DFF0 (nQ)	. . .	LOGIC_1
OUT	#	0	1	2	3	4	5	. . .	. . .	. . .	27	. . .	31
IO3 <4:0>	0												
IO4 <9:5>	1												
IO4 (DIR) <14:10>	2												
DFF0(CLK) <20:16>	3												
DFF0(D) <25:21>	4												
2-bit LUT1(IN0) <30:26>	5												
. .	. .												
. .	. .												
. .	. .												
IO6 <190:186>	36												
IO7 <196:192>	37												
IO8 <201:197>	38												
IO8(DIR) <206:202>	39												

Figure 6.2. Connection Matrix Structure

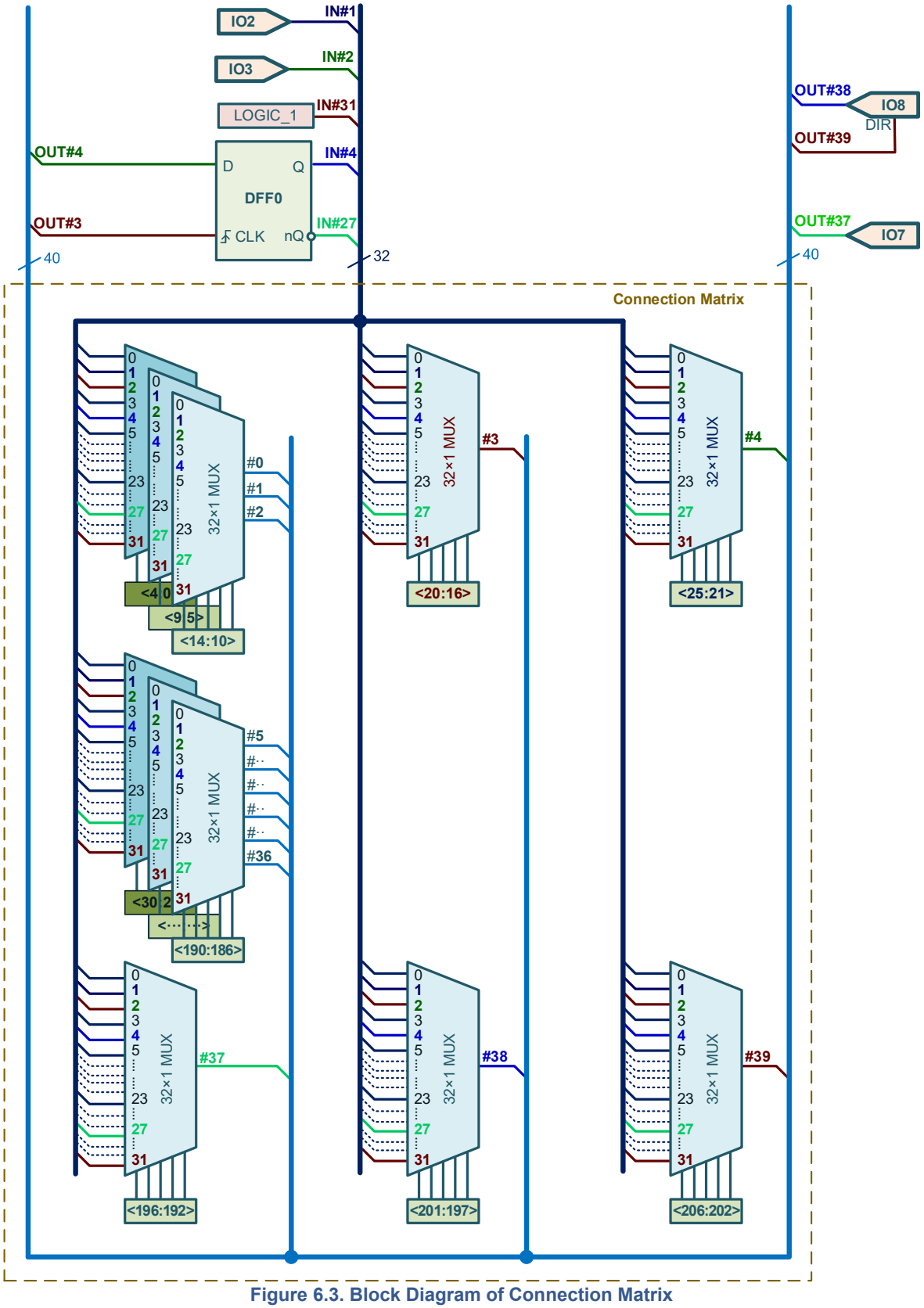


Figure 6.3. Block Diagram of Connection Matrix

6.2. Matrix Input Table

Table 6.1. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
00	Logic 0	0	0	0	0	0
01	IO2 DOUT	0	0	0	0	1
02	IO3 DOUT	0	0	0	1	0
03	IO4 DOUT	0	0	0	1	1
04	MF0(2-bit LUT0 / DFF0/LATCH0) OUT / Q	0	0	1	0	0
05	MF1(2-bit LUT1 / DFF1/LATCH1) OUT / Q	0	0	1	0	1
06	2-bit LUT2 OUT	0	0	1	1	0
07	2-bit LUT3 OUT	0	0	1	1	1
08	MF2(3-bit LUT0 / DFF2/LATCH2) OUT0 / Q	0	1	0	0	0
09	MF3(3-bit LUT1 / DFF3/LATCH3) OUT0 / Q	0	1	0	0	1
10	MF4(3-bit LUT2 / DFF4/LATCH4) OUT / Q	0	1	0	1	0
11	MF5(3-bit LUT3 / DFF5/LATCH5) OUT / Q	0	1	0	1	1
12	MF6(3-bit LUT4 / Shift Register) OUT0	0	1	1	0	0
13	MF6(3-bit LUT4 / Shift Register) OUT1/nOUT1	0	1	1	0	1
14	MF8(4-bit LUT0 / 16-bit TMR2) OUT	0	1	1	1	0
15	8-bit TMR0 OUT	0	1	1	1	1
16	8-bit TMR1 OUT	1	0	0	0	0
17	8-bit TMR3 OUT	1	0	0	0	1
18	8-bit TMR3 ED	1	0	0	1	0
19	MF7(PDLY / Edge Detector) OUT/nOUT	1	0	0	1	1
20	MF6(3-bit LUT8/ Shift Register) OUT2(LUT)/Q[1]	1	0	1	0	0
21	OSC OUT1	1	0	1	0	1
22	OSC OUT0	1	0	1	1	0
23	Ready	1	0	1	1	1
24	IO6 DOUT	1	1	0	0	0
25	IO7 DOUT	1	1	0	0	1
26	IO8 DOUT	1	1	0	1	0
27	MF0(2-bit LUT0 / DFF0/LATCH0) nQ	1	1	0	1	1
28	MF1(2-bit LUT1 / DFF1/LATCH1) nQ	1	1	1	0	0
29	MF2(3-bit LUT0 / DFF2/LATCH2) OUT1 / nQ	1	1	1	0	1
30	MF3(3-bit LUT1 / DFF3/LATCH3) OUT1 / nQ	1	1	1	1	0
31	Logic 1	1	1	1	1	1

6.3. Matrix Output Table

Table 6.2. Matrix Output Table

Register Bit Address	Register Name	Register Definition
Connection matrix outputs		
<4:0>	CMO0_IO3_DIN	IO3 DIN
<9:5>	CMO1_IO4_DIN	IO4 DIN
<14:10>	CMO2_IO4_DIR	IO4 DIR
<20:16>	CMO3_MF0_2BLUT0_DFF0_IN0_CLK	MF0(2-bit LUT0/DFF0/LATCH0) IN0/CLK/nL
<25:21>	CMO4_MF0_2BLUT0_DFF0_IN1_D	MF0(2-bit LUT0/DFF0/LATCH0) IN1/D
<30:26>	CMO5_MF1_2BLUT1_DFF1_IN0_CLK	MF1(2-bit LUT1/DFF1/LATCH1) IN0/CLK/nL
<35:31>	CMO6_MF1_2BLUT1_DFF1_IN1_D	MF1(2-bit LUT1/DFF1LATCH1) IN1/D
<40:36>	CMO7_2BLUT2_IN0	2-bit LUT2 IN0
<48:44>	CMO8_2BLUT2_IN1	2-bit LUT2 IN1
<53:49>	CMO9_2BLUT3_IN0	2-bit LUT3 IN0
<58:54>	CMO10_2BLUT3_IN1	2-bit LUT3 IN1
<63:59>	CMO11_MF2_3BLUT0_DFF2_IN0_CLK	MF2(3-bit LUT0/DFF2/LATCH2) IN0/CLK/nL
<68:64>	CMO12_MF2_3BLUT0_DFF2_IN1_D	MF2(3-bit LUT0/DFF2/LATCH2) IN1/D
<73:69>	CMO13_MF2_3BLUT0_DFF2_IN2_NRST	MF2(3-bit LUT0/DFF2/LATCH2) IN2/nRST
<78:74>	CMO14_MF3_3BLUT1_DFF3_IN0_CLK	MF3(3-bit LUT1/DFF3/LATCH3) IN0/CLK/nL
<83:79>	CMO15_MF3_3BLUT1_DFF3_IN1_D	MF3(3-bit LUT1/DFF3/LATCH3) IN1/D
<89:85>	CMO16_MF3_3BLUT1_DFF3_IN2_NRST	MF3(3-bit LUT1/DFF3/LATCH3) IN2/nRST
<94:90>	CMO17_MF4_3BLUT2_DFF4_IN0_CLK	MF4(3-bit LUT2/DFF4/LATCH4) IN0/CLK/nL
<99:95>	CMO18_MF4_3BLUT2_DFF4_IN1_D	MF4(3-bit LUT2/DFF4/LATCH4) IN1/D
<104:100>	CMO19_MF4_3BLUT2_DFF4_IN2_NRST	MF4(3-bit LUT2/DFF4/LATCH4) IN2/nRST
<109:105>	CMO20_MF5_3BLUT3_DFF5_IN0_CLK	MF5(3-bit LUT3/DFF5/LATCH5) IN0/CLK/nL
<114:110>	CMO21_MF5_3BLUT3_DFF5_IN1_D	MF5(3-bit LUT3/DFF5/LATCH5) IN1/D
<119:115>	CMO22_MF5_3BLUT3_DFF5_IN2_NRST	MF5(3-bit LUT3/DFF5/LATCH5) IN2/nRST
<124:120>	CMO23_MF6_3BLUT4_SH_REG_IN0_D	MF6(3-bit LUT4/Shift Register) IN0/D
<129:125>	CMO24_MF6_3BLUT4_SH_REG_IN1_NRST	MF6(3-bit LUT4/Shift Register) IN1/nRST
<134:130>	CMO25_MF6_3BLUT4_SH_REG_IN2_CLK	MF6(3-bit LUT4/Shift Register) IN2/CLK
<139:135>	CMO26_MF8_4BLUT0_16BTMR2_IN0_CLK	MF8(4-bit LUT0/16-bit TMR2) IN0/CLK
<145:141>	CMO27_MF8_4BLUT0_16BTMR2_IN1_RST	MF8(4-bit LUT0/16-bit TMR2) IN1/RST
<150:146>	CMO28_MF8_4BLUT0_16BTMR2_IN2_KEEP	MF8(4-bit LUT0/16-bit TMR2) IN2/KEEP
<155:151>	CMO29_MF8_4BLUT0_16BTMR2_IN3_UP	MF8(4-bit LUT0/16-bit TMR2) IN3/UP
<160:156>	CMO30_8BTMR0_IN_RST	8-bit TMR0 IN/RST
<165:161>	CMO31_8BTMR1_IN_RST	8-bit TMR1 IN/RST
<170:166>	CMO32_8BTMR0_8BTMR1_CLK	8-bit TMR0/8-bit TMR1 CLK
<175:171>	CMO33_8BTMR3_IN_CLK	8-bit TMR3 IN/CLK
<180:176>	CMO34_MF7_PDLY_ED_IN	MF7(PDLY/Edge Detector) IN
<185:181>	CMO35_OSC_PWR_DWN	OSC PWR DWN
<190:186>	CMO36_IO6_DIN	IO6 DIN
<196:192>	CMO37_IO7_DIN	IO7 DIN
<201:197>	CMO38_IO8_DIN	IO8 DIN
<206:202>	CMO39_IO8_DIR	IO8 DIR

7. Combinatorial Logic

Two Look Up Tables (LUTs) within the AM1U1108 provide the support for combinatorial logic. There are two 2-bit LUTs, and there are eight Multifunctional Macrocells that can be used as LUTs. For more details, please see Section 8 Multifunctional Macrocells.

7.1. 2-bit LUT

The 2-bit LUT (Figure 7.1) takes in two input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 7.1.

Table 7.1. Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

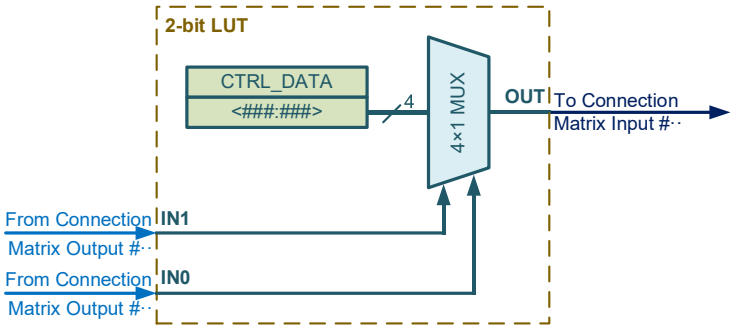


Figure 7.1. 2-bit LUTs

7.1.1. 2-bit LUT2 Macrocell

Registers of 2-bit LUT2 defined its output function set out in Table 7.2.

Table 7.2. 2-bit LUT2 Truth Table

Register Bit Address	Register Name	Register Definition
2-bit LUT2		
<230:227>	2BLUT2_CTRL_DATA	OUT LUT control data

7.1.2. 2-bit LUT3 Macrocell

Registers of 2-bit LUT3 defined its output function set out in Table 7.3).

Table 7.3. 2-bit LUT3 Truth Table

Register Bit Address	Register Name	Register Definition
2-bit LUT0		
<234:231>	2BLUT2_CTRL_DATA	OUT LUT control data

8. Multifunctional Macrocells

Nine multifunction macrocells (MF) in the AM1U1108 can serve more than one logic or timing function. They can serve as a Look Up Table (LUT) or as another logic or timing function in four of the cases. Functions that can be implemented in these macrocells:

- Two selectable 2-bit LUTs or DFF/LATCHs;
- Four selectable 3-bit LUTs or DFF/LATCHs;
- One 3-bit LUT or 16-bit Shift Register;
- One 4-bit LUT or 8-Bit TMR;
- One Programmable Delay or Edge Detector.

8.1. MF (2-bit LUT / DFF/LATCH) Macrocells

The AM1U1108 has MF macrocells capable of serving as either 2-bit LUTs, DFFs or LATCHs (see Figure 8.1).

When the MF macrocells are used as LUT, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, that goes back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 8.1.

When the macrocells are used as DFF or LATCH, the two input signals from the connection matrix go to the data (D) and clock/nlatch (CLK/nL) inputs for the DFF/LATCH, and the outputs Q and nQ go back to the connection matrix. Operation of the DFF and LATCH are shown in the Table 8.2, Table 8.3.

Table 8.1. 2-bit LUT Truth Table of Standard Logic Gates

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0

Table 8.2. Operation of the DFF

D	CLK	Q(t)/nQ(t)
0	⤓	0/1
0	⤒	t–1
1	⤓	1/0
1	⤒	t–1

Note 8.1: X – Don't Care
Note 8.2: t–1 – Previous State

Table 8.3. Operation of the LATCH

nL	D	Q(t)/nQ(t)
0	0	t–1
0	1	t–1
1	0	0/1
1	1	1/0

Note 8.3: X – Don't Care
Note 8.4: t–1 – Previous State

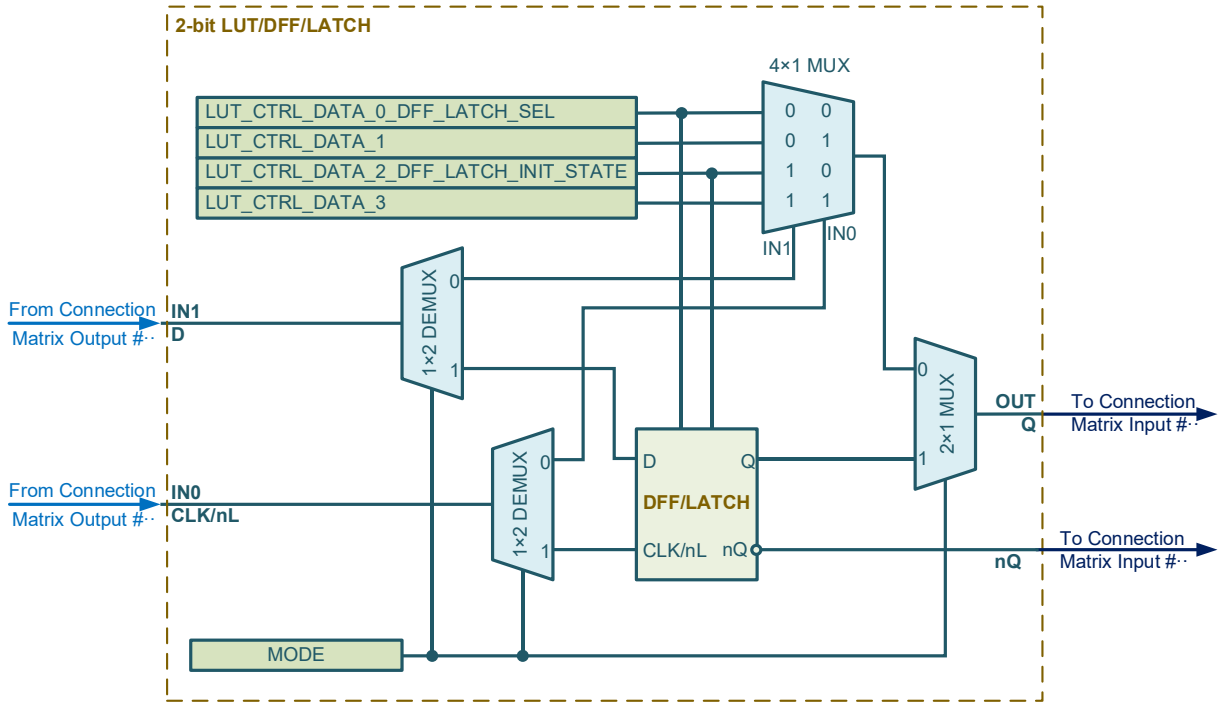


Figure 8.1. Schematic diagram of mf (2-bit LUT/DFF/LATCH)

8.1.1. MF0 (2-bit LUT0/DFF0/LATCH0) Macrocell

Register settings of MF0 (2-bit LUT0/DFF0/LATCH0) macrocell set out in Table 8.4.

Table 8.4. MF0 (2-bit LUT0/DFF0/LATCH0) Register Settings

Register Bit Address	Register Name	Register Definition
MF0 (2-bit LUT0/DFF0/LATCH0)		
<235>	MF0_MODE	MF mode: 0: LUT 1: DFF/LATCH
<215>	MF0_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<216>	MF0_LUT_CTRL_DATA_1	1st bit of LUT control data: 0: LOW 1: HIGH
<217>	MF0_LUT_CTRL_DATA_2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<218>	MF0_LUT_CTRL_DATA_3	3rd bit of LUT control data: 0: LOW 1: HIGH

The MF0 (2-bit LUT0/DFF0/LATCH0) macrocell, if programmed for a LUT function, uses 4-bit register to define its output function by reg<218:215> (see Table 8.5).

Table 8.5. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	MF0_LUT_CTRL_DATA_0_DFF_LATCH_SEL	LSB
0	1	MF0_LUT_CTRL_DATA_1	
1	0	MF0_LUT_CTRL_DATA_2_DFF_LATCH_INIT_STATE	
1	1	MF0_LUT_CTRL_DATA_3	MSB

8.1.2. MF1 (2-bit LUT1/DFF1/LATCH1) Macrocell

Register settings of MF1 (2-bit LUT1/DFF1/LATCH1) macrocell set out in Table 8.6.

Table 8.6. MF1 (2-bit LUT1/DFF1/LATCH1) Register Settings

Register Bit Address	Register Name	Register Definition
MF1 (2-bit LUT1/DFF1/LATCH1)		
<236>	MF1_MODE	MF mode: 0: LUT 1: DFF/LATCH
<220>	MF1_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<221>	MF1_LUT_CTRL_DATA_1	1st bit of LUT control data: 0: LOW 1: HIGH
<222>	MF1_LUT_CTRL_DATA_2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<223>	MF1_LUT_CTRL_DATA_3	3rd bit of LUT control data: 0: LOW 1: HIGH

The MF1 (2-bit LUT1/DFF1/LATCH1) macrocell, if programmed for a LUT function, uses 4-bit register to define its output function by reg<223:220> (see Table 8.7).

Table 8.7. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	MF1_LUT_CTRL_DATA_0_DFF_LATCH_SEL	LSB
0	1	MF1_LUT_CTRL_DATA_1	
1	0	MF1_LUT_CTRL_DATA_2_DFF_LATCH_INIT_STATE	
1	1	MF1_LUT_CTRL_DATA_3	MSB

8.2. MF (3-bit LUT / DFF/LATCH) Macrocells

The AM1U1108 has a MF macrocell that can serve as either 3-bit LUTs or as DFF/LATCHs (Figure 8.2, Figure 8.3).

When the MF macrocells are used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output for 3-bit LUT2 and 3-bit LUT3, and two outputs for 3-bit LUT0 and 3-bit LUT1, that go back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 8.8.

When the macrocells are used as DFF or LATCH, the three input signals from the connection matrix go to the data (D), clock/nlatch (CLK/nL) and (n)RST/(n)SET inputs of the DFF/LATCH, and the output(DFF4/LATCH4, DFF5/LATCH5) or outputs(DFF2/LATCH2, DFF3/LATCH3) go back to the connection matrix. Operation of the DFF and LATCH are shown in the Table 8.9, Table 8.10.

Table 8.8. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

Table 8.9. Operation of the DFF

nRST/nSET	D	CLK	Q(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	↓	0/1
1	0	↑	t–1
1	1	↓	1/0
1	1	↑	t–1

Note 8.5: X – Don't Care
Note 8.6: t–1 – Previous State

Table 8.10. Operation of the LATCH

nRST/nSET	nL	D	Q(t)/nQ(t)
nRST = 0	X	X	0/1
nSET = 0	X	X	1/0
1	0	0	t–1
1	0	1	t–1
1	1	0	0/1
1	1	1	1/0

Note 8.7: X – Don't Care
Note 8.8: t–1 – Previous State

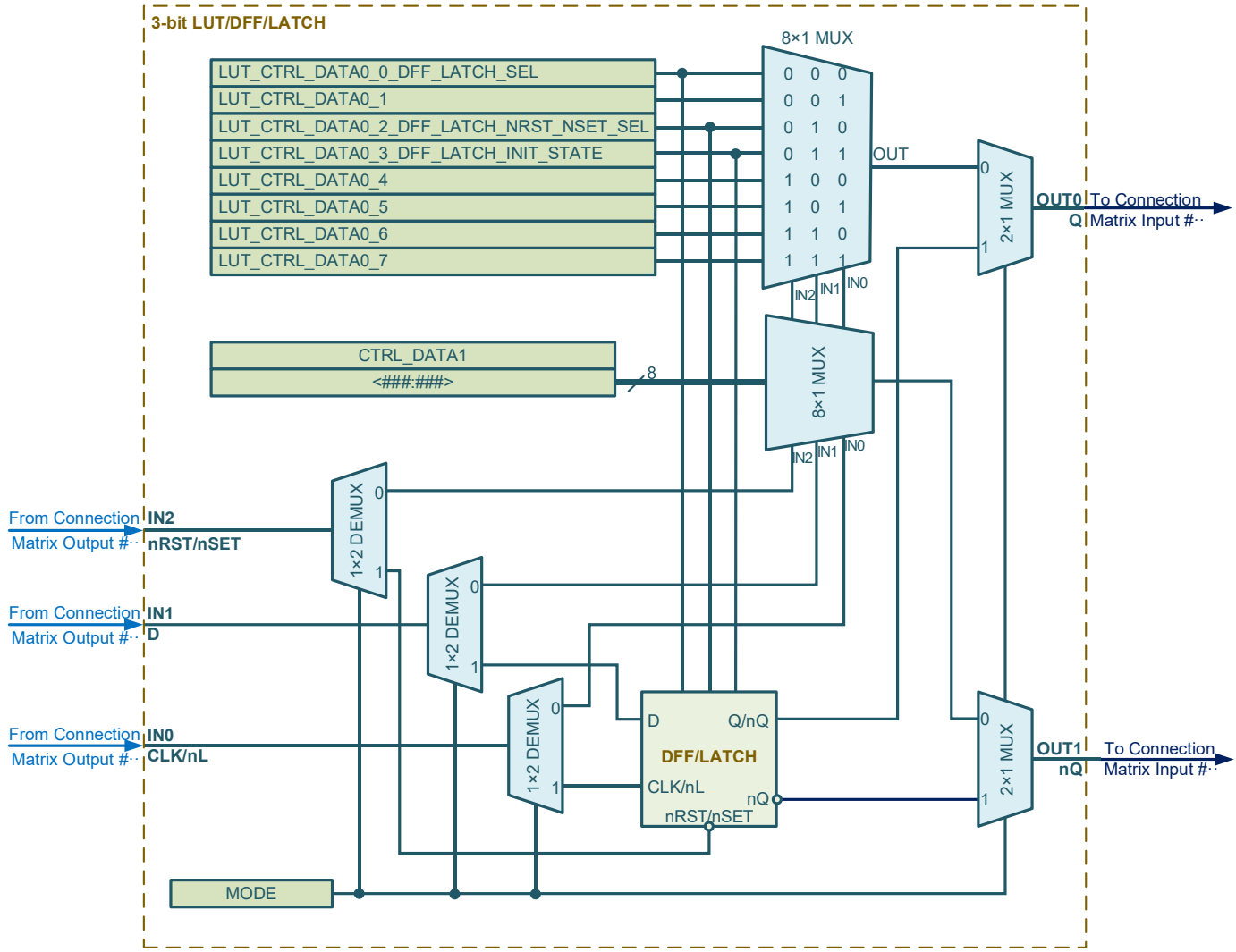


Figure 8.2. Schematic diagram of MF (3-bit LUT/DFF/LATCH) (with 2 OUTs and nRST/nSET)

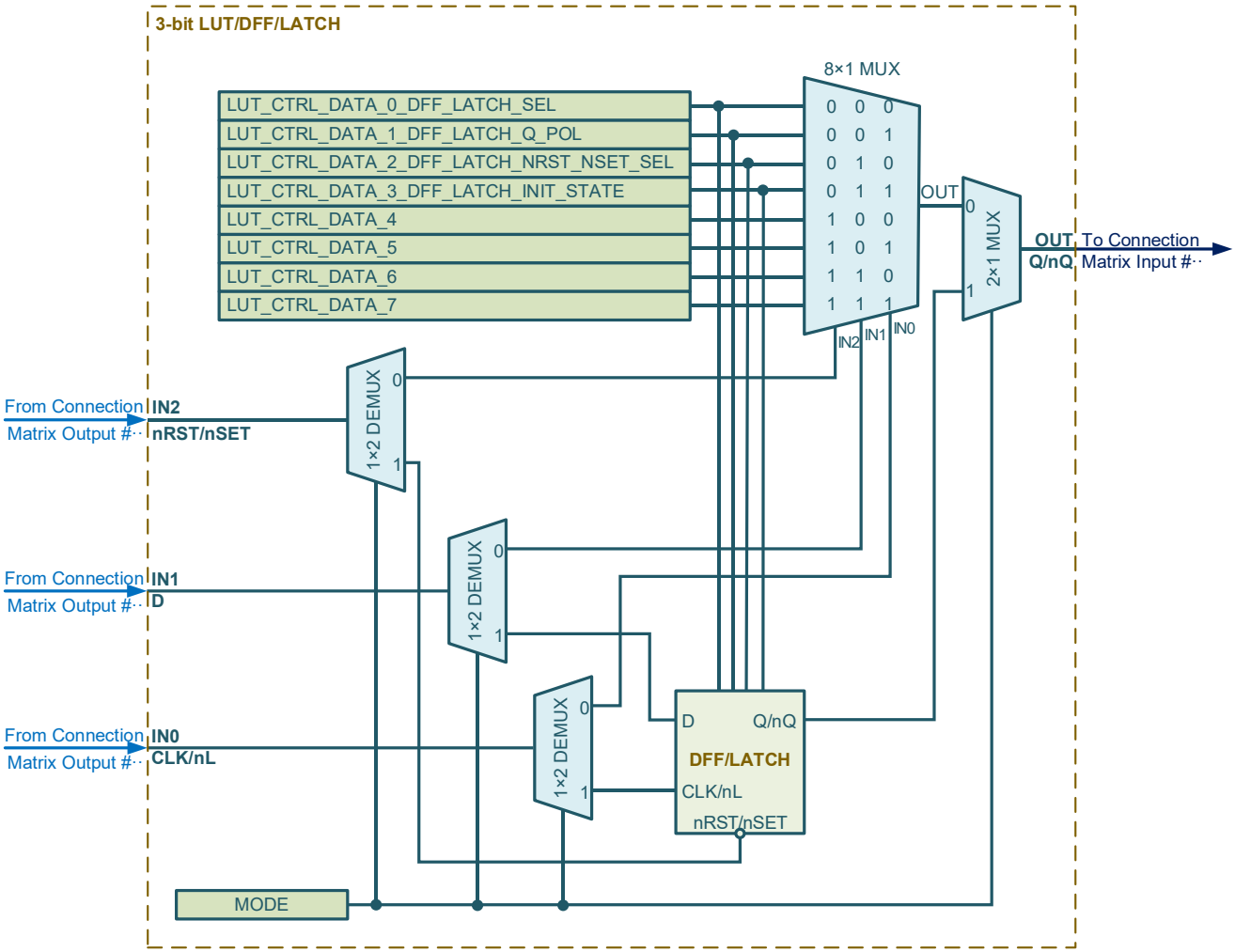


Figure 8.3. Schematic diagram of MF (3-bit LUT/DFF/LATCH) (with single OUT and nRST/nSET)

8.2.1. MF2 (3-bit LUT0/DFF2/LATCH2)

Schematic diagram of MF2 (3-bit LUT0/DFF2/LATCH2) macrocell is shown in Figure 8.2. Its register settings set out in Table 8.11.

Table 8.11. MF2 (3-bit LUT0/DFF2/LATCH2) Register Settings

Register Bit Address	Register Name	Register Definition
MF2 (3-bit LUT0/DFF2/LATCH2)		
<293>	MF2_MODE	MF mode: 0: LUT 1: DFF/LATCH
<237>	MF2_LUT_CTRL_DATA0_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<238>	MF2_LUT_CTRL_DATA0_1	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH
<239>	MF2_LUT_CTRL_DATA0_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<240>	MF2_LUT_CTRL_DATA0_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<241>	MF2_LUT_CTRL_DATA0_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<242>	MF2_LUT_CTRL_DATA0_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<243>	MF2_LUT_CTRL_DATA0_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<244>	MF2_LUT_CTRL_DATA0_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<252:245>	MF2_LUT_CTRL_DATA1	OUT1 LUT control data

The MF2 (3-bit LUT0/DFF2/LATCH2) macrocell, if programmed for a LUT function, uses 8-bit register to define its output function (see Table 8.12):

OUT0 by reg<244:237>;
OUT1 by reg<252:245>.

Table 8.12. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT0	OUT0	
0	0	0	MF2_LUT_CTRL_DATA0_0_DFF_LATCH_SEL	MF2_CTRL_DATA1<0>	LSB
0	0	1	MF2_LUT_CTRL_DATA0_1	MF2_CTRL_DATA1<1>	
0	1	0	MF2_LUT_CTRL_DATA0_2_DFF_LATCH_NRST_NSET_SEL	MF2_CTRL_DATA1<2>	
0	1	1	MF2_LUT_CTRL_DATA0_3_DFF_LATCH_INIT_STATE	MF2_CTRL_DATA1<3>	
1	0	0	MF2_LUT_CTRL_DATA0_4	MF2_CTRL_DATA1<4>	
1	0	1	MF2_LUT_CTRL_DATA0_5	MF2_CTRL_DATA1<5>	
1	1	0	MF2_LUT_CTRL_DATA0_6	MF2_CTRL_DATA1<6>	
1	1	1	MF2_LUT_CTRL_DATA0_7	MF2_CTRL_DATA1<7>	MSB

8.2.2. MF3 (3-bit LUT1/DFF3/LATCH3)

Schematic diagram of MF3 (3-bit LUT1/DFF3/LATCH3) macrocell is shown in Figure 8.2. Its register settings set out in Table 8.13.

Table 8.13. MF3 (3-bit LUT1/DFF3/LATCH3) Register Settings

Register Bit Address	Register Name	Register Definition
MF3 (3-bit LUT1/DFF3/LATCH3)		
<294>	MF3_MODE	MF mode: 0: LUT 1: DFF/LATCH
<253>	MF3_LUT_CTRL_DATA0_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<254>	MF3_LUT_CTRL_DATA0_1	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH
<255>	MF3_LUT_CTRL_DATA0_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<256>	MF3_LUT_CTRL_DATA0_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<257>	MF3_LUT_CTRL_DATA0_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<258>	MF3_LUT_CTRL_DATA0_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<259>	MF3_LUT_CTRL_DATA0_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<260>	MF3_LUT_CTRL_DATA0_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<268:261>	MF3_LUT_CTRL_DATA1	OUT1 LUT control data

The MF3 (3-bit LUT1/DFF3/LATCH3) macrocell, if programmed for a LUT function, uses 8-bit register to define its output function (see Table 8.14):

OUT0 by reg<260:253>;
OUT1 by reg<268:261>.

Table 8.14. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT0	OUT0	
0	0	0	MF3_LUT_CTRL_DATA0_0_DFF_LATCH_SEL	MF3_CTRL_DATA1<0>	LSB
0	0	1	MF3_LUT_CTRL_DATA0_1	MF3_CTRL_DATA1<1>	
0	1	0	MF3_LUT_CTRL_DATA0_2_DFF_LATCH_NRST_NSET_SEL	MF3_CTRL_DATA1<2>	
0	1	1	MF3_LUT_CTRL_DATA0_3_DFF_LATCH_INIT_STATE	MF3_CTRL_DATA1<3>	
1	0	0	MF3_LUT_CTRL_DATA0_4	MF3_CTRL_DATA1<4>	
1	0	1	MF3_LUT_CTRL_DATA0_5	MF3_CTRL_DATA1<5>	
1	1	0	MF3_LUT_CTRL_DATA0_6	MF3_CTRL_DATA1<6>	
1	1	1	MF3_LUT_CTRL_DATA0_7	MF3_CTRL_DATA1<7>	MSB

8.2.3. MF4 (3-bit LUT2/DFF4/LATCH4)

Schematic diagram of MF4 (3-bit LUT2/DFF4/LATCH4) macrocell is shown in Figure 8.3. Its register settings set out in Table 8.15.

Table 8.15. MF4 (3-bit LUT2/DFF4/LATCH4) Register Settings

Register Bit Address	Register Name	Register Definition
MF4 (3-bit LUT2/DFF4/LATCH4)		
<295>	MF4_MODE	MF mode: 0: LUT 1: DFF/LATCH
<269>	MF4_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<270>	MF4_LUT_CTRL_DATA_1_Q_POL	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<271>	MF4_LUT_CTRL_DATA_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<272>	MF4_LUT_CTRL_DATA_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<273>	MF4_LUT_CTRL_DATA_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<274>	MF4_LUT_CTRL_DATA_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<275>	MF4_LUT_CTRL_DATA_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<276>	MF4_LUT_CTRL_DATA_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH

The MF4 (3-bit LUT2/DFF4/LATCH4) macrocell, if programmed for a LUT function, uses 8-bit register to define its output function by reg<276:269> (see Table 8.16).

Table 8.16. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF4_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	0	1	MF4_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
0	1	0	MF4_LUT_CTRL_DATA2_DFF_LATCH_NRST_NSET_SEL	
0	1	1	MF4_LUT_CTRL_DATA3_DFF_LATCH_INIT_STATE	
1	0	0	MF4_LUT_CTRL_DATA4_DFF_LATCH	
1	0	1	MF4_LUT_CTRL_DATA_5	
1	1	0	MF4_LUT_CTRL_DATA_6	
1	1	1	MF4_LUT_CTRL_DATA_7	MSB

8.2.4. MF5 (3-bit LUT3/DFF5/LATCH5)

Schematic diagram of 3-bit MF5 (LUT3/DFF5/LATCH5) macrocell is shown in Figure 8.3. Its register settings set out in Table 8.21.

Table 8.17. MF5 (3-bit LUT3/DFF5/LATCH5) Register Settings

Register Bit Address	Register Name	Register Definition
MF5 (3-bit LUT3/DFF5/LATCH5)		
<296>	MF5_MODE	MF mode: 0: LUT 1: DFF/LATCH
<277>	MF5_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<278>	MF5_LUT_CTRL_DATA_1_Q_POL	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<279>	MF5_LUT_CTRL_DATA_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<280>	MF5_LUT_CTRL_DATA_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<281>	MF5_LUT_CTRL_DATA_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<282>	MF5_LUT_CTRL_DATA_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<283>	MF5_LUT_CTRL_DATA_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<284>	MF5_LUT_CTRL_DATA_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH

The MF5 (3-bit LUT3/DFF5/LATCH5) macrocell, if programmed for a LUT function, uses 8-bit register to define its output function by reg<284:277> (see Table 8.18).

Table 8.18. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF5_LUT_CTRL_DATA0_DFF_LATCH_SEL	LSB
0	0	1	MF5_LUT_CTRL_DATA1_DFF_LATCH_Q_POL	
0	1	0	MF5_LUT_CTRL_DATA2_DFF_LATCH_NRST_NSET_SEL	
0	1	1	MF5_LUT_CTRL_DATA3_DFF_LATCH_INIT_STATE	
1	0	0	MF5_LUT_CTRL_DATA4_DFF_LATCH	
1	0	1	MF5_LUT_CTRL_DATA_5	
1	1	0	MF5_LUT_CTRL_DATA_6	
1	1	1	MF5_LUT_CTRL_DATA_7	MSB

8.3. MF (3-bit LUT/Shift Register) Macrocell

The MF macrocell has a capability to serve as either a 3-bit LUT or as a Shift Register (SHR).

When the MF macrocell is used as LUT, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, that go back into the connection matrix. The LUT allows to implement user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT is shown in the Table 8.19.

The Shift Register contains sixteen stages cascade of positive edge triggered DFFs. The signal from any stage can be routed to OUT0 and OUT1 independently. The Q[1] output is always connected to the output of the first stage. The Shift Register has Data (D), Clock (CLK) and Reset (nRST) inputs from connection matrix. Applying low-level signal to the nRST sets all stage values to zero.

Schematic diagram of 3-bit LUT4/Shift Register macrocell is shown on Figure 8.4.

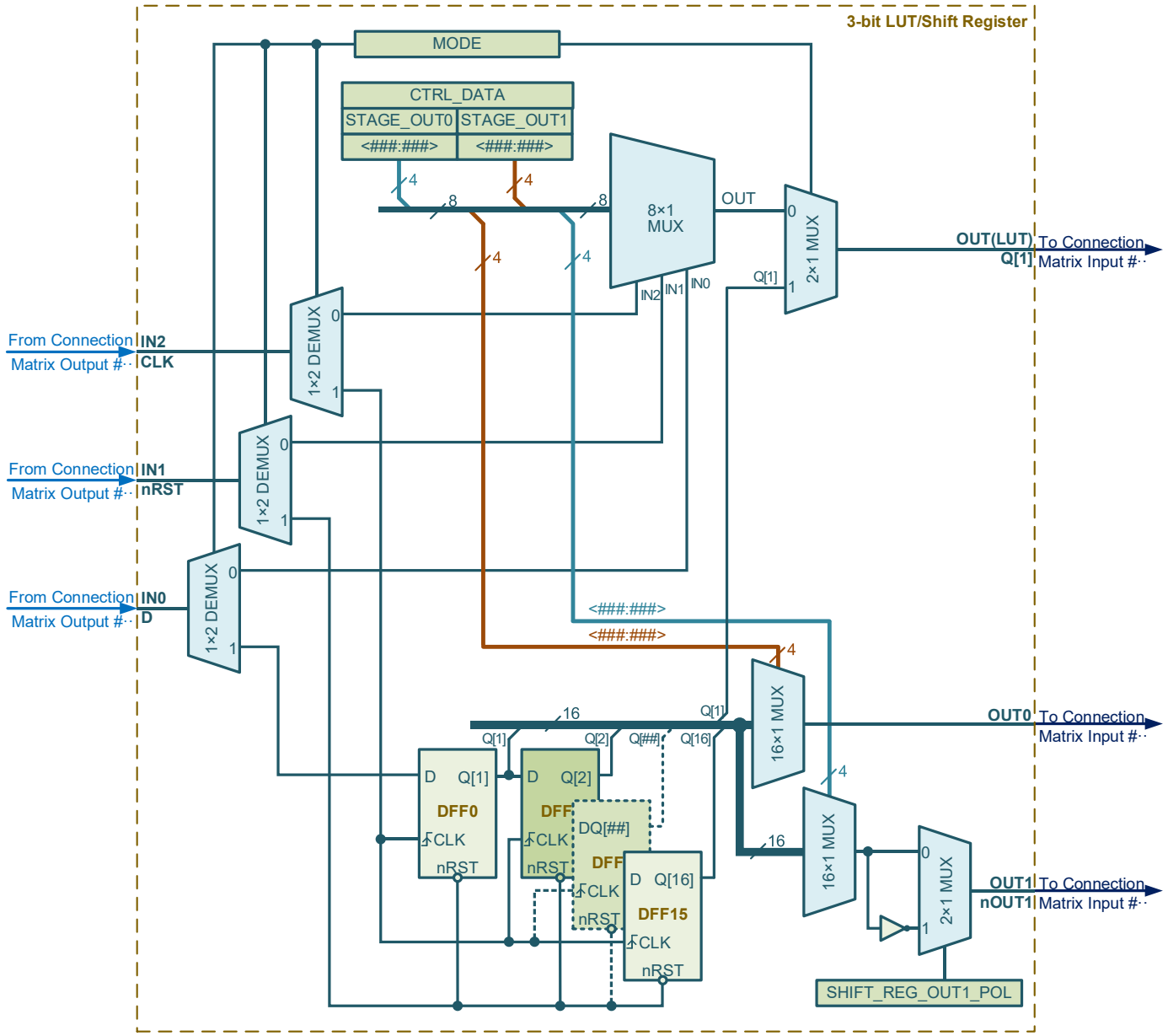


Figure 8.4. 3-bit LUT4/Shift Register

Table 8.19. 3-bit LUT Truth Table of Standard Logic Gates

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

8.3.1. MF6 (3-bit LUT4/Shift Register)

The MF registers set out in Table 8.20.

Table 8.20. MF6 (3-bit LUT4/Shift Register) Registers Settings

Register Bit Address	Register Name	Register Definition
MF6 (3-bit LUT4/Shift Register)		
<297>	MF6_MODE	MF mode: 0: LUT 1: Shift register
<298>	MF6_SHIFT_REG_OUT1_POL	Shift register OUT1 polarity: 0: OUT1 1: nOUT1
<288:285>	MF6_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0	Low tetrad of OUT LUT control data or stage of OUT0 shift register
<292:289>	MF6_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1	High tetrad of OUT LUT control data or stage of OUT1 shift register

The MF6 (3-bit LUT4/Shift Register) macrocell, if programmed for a LUT function, uses 8-bit register to define its output function by reg<292:285> (see Table 8.21).

Table 8.21. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	MF6_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<0>	LSB
0	0	1	MF6_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<1>	
0	1	0	MF6_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<2>	
0	1	1	MF6_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0<3>	
1	0	0	MF6_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<0>	
1	0	1	MF6_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<1>	
1	1	0	MF6_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<2>	
1	1	1	MF6_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1<3>	MSB

8.4. MF (PDLY/Edge Detector) - Programmable Delay/Edge Detector Macrocell

The AM1U1108 has a macrocell that can serve as programmable delay (PDLY) or as edge detector (Figure 8.5).

In the PDLY mode the macrocell serves as both edge delay with four selectable delay value T_{ADJ}: 140 ns, 280 ns, 420 ns, 560 ns. If input signal is shorter than the delay value, the signal does not propagate to the output and is filtered out.

In the Edge Detector mode, the macrocell generates a high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The pulse width value (T_{WIDTH}) is configurable (140 ns, 280 ns, 420 ns, 560 ns). See the timing diagrams below for further information (Figure 8.6).

The output polarity of the macrocell is configurable and can be selected as non-inverted or inverted.

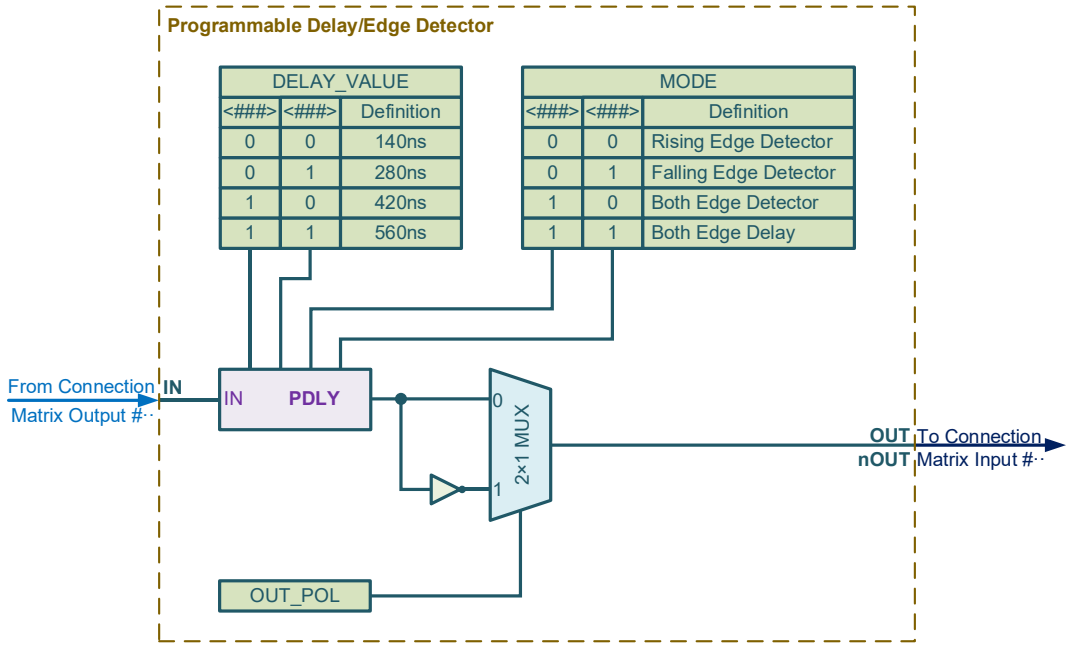


Figure 8.5. Programmable Delay

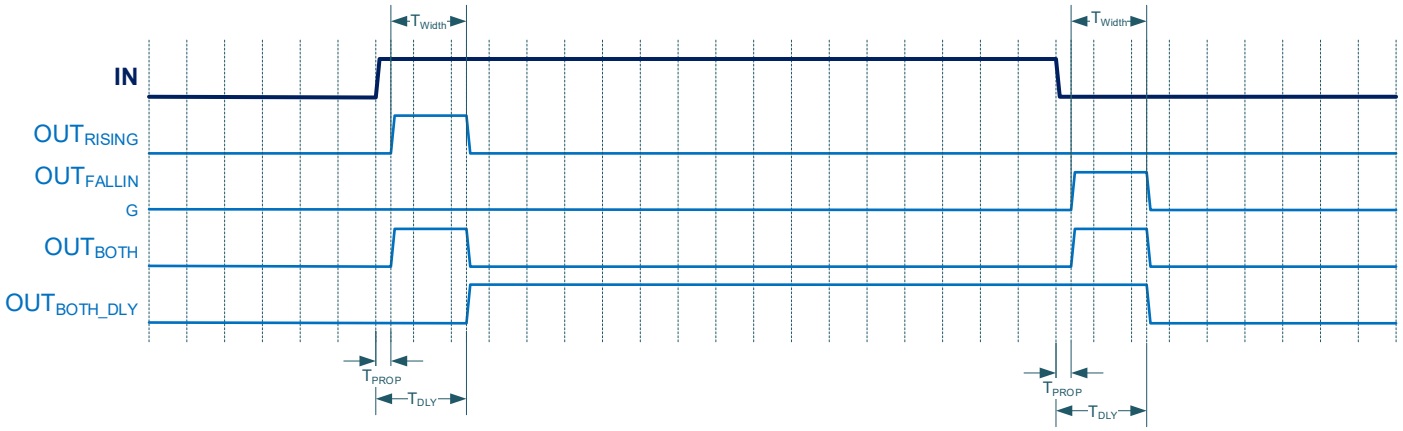


Figure 8.6. Edge Detector Output

8.4.1. MF7 (PDLY/Edge Detector)

Settings of MF7 (PDLY/Edge Detector) is shown in Table 8.22.

Table 8.22. MF7 (PDLY/Edge Detector) Register Settings

Register Bit Address	Register Name	Register Definition
MF7 (PDLY/Edge Detector)		
<458>	MF7_OUT_POL	Output polarity: 0: OUT 1: nOUT
<460:459>	MF7_MODE	MF mode: 00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
<462:461>	MF7_DELAY_VAL	Delay value: 00: 140ns 01: 280ns 10: 420ns 11: 560ns

8.5. MF (4-bit LUT0/16-Bit Timer) Macrocells

One macrocell has the capability to serve as 4-bit LUTs or as 16-bit timer (TMR) (Figure 8.7).

When the MF macrocell is configured as LUT, the 4-bit LUT receives four input signals from the connection matrix and generates a single output, which is routed back into the connection matrix. The LUT allows the implementation of user-defined combinatorial logic function, including standard digital logic gates (AND, NAND, OR, NOR, XOR, XNOR). Standard logic gates configuration of the LUT are shown in the Table 8.23.

When the macrocell is configured as 16-bit TMR, four input signals from the connection matrix go to the external clock (EXTCLK), IN (RST for Counter mode), KEEP and UP. The output signal is routed back to the connection matrix.

The timer has the following mode of operation:

- Delay
- Counter
- One Shot
- Frequency Detector

The output polarity of the TMR is configurable and can be selected as non-inverted or inverted.

The KEEP input allows to pause counting by applying HIGH level to KEEP, the counting is resume after KEEP goes LOW.

In the Delay mode the TMR delays the input signal by the selected edge event (rising edge, falling edge, both edges) for a time determined by the Control Data, input clock signal and selected divider value. If input signal is shorter than the delay value, the signal does not propagate to the output. The timing diagrams of this mode is shown in the Figure 9.1…Figure 9.6.

In the Counter mode the TMR divides input clock signal by the value determined by the Control Data, input clock signal and selected divider value. The output of the TMR goes HIGH every time when the Counted Value (current value of the counter) is equal 0. The RST in of the TMR reset Counted value to 0 by one of the following events: rising edge, falling edge, both edge, high level. The timing diagrams of this mode is shown in the Figure 9.7…Figure 9.12.

The TMR2 also support Up/Down counting mode. By default, the counter decrements. The counting direction reverses when a HIGH level is applied to the UP input. Counting can be paused by applying a HIGH level to the KEEP input. The count resumes when the level goes LOW. Timing diagrams of the Up/Down mode are shown in Figure 9.32…Figure 9.35.

In One-Shot mode this macrocell generates a high-level pulse with a set width, when detecting the edge event, which is selectable by the registers, on its IN input. The pulse width is determined by the Control Data, input clock signal and selected divider value. Any incoming edges are ignored during pulse width generation. The timing diagrams of this mode is shown in the Figure 9.13…Figure 9.18.

In Frequency Detector mode the TMR function following scenarios:

- Rising Edge: The output will go HIGH if the time between two rising edges is less than the delay.
  The output will go LOW if the next rising edge has not come after the last rising edge in specified time.
- Falling Edge: The output will go HIGH if the time between two falling edges is less than the set time.
  The output will go LOW if the next falling edge has not come after the last falling edge in specified time.
- Both Edges: The output will go HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse.
  The output will go LOW if the next rising/falling edge has not come after the last falling/rising edge in specified time.

The timing diagrams of the Frequency Detector Mode is shown in the Figure 9.19…Figure 9.24.

Time of Timers for each mode can be calculated using the following formulas (Note 8.9, Note 10):

- Delay (Figure 9.1…Figure 9.6)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK};
- Counter Figure 9.7…Figure 9.12, Figure 9.32…Figure 9.35)
  Output Period = (Control Data + 1)/F_{CLK};
  Output Frequency = F_{CLK}/(Control Data + 1);
- One Shot (Figure 9.13…Figure 9.18)
  Pulse width = (Control Data + 1 + VAR)/F_{CLK};
- Frequency Detector (Figure 9.19…Figure 9.24)
  Detected Frequency = F_{CLK}/(Control Data + 1 + VAR).

Note 8.9 *F_{CLK} – CLK input frequency.*

Note 8.10 *VAR = 0…1 – defined by the asynchronous time between the input signal and the first clock pulse.*

Note 8.11 *Counters initialize with Control Data after POR.*

Table 8.23. 4-bit LUT Truth Table of Standard Logic Gates

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

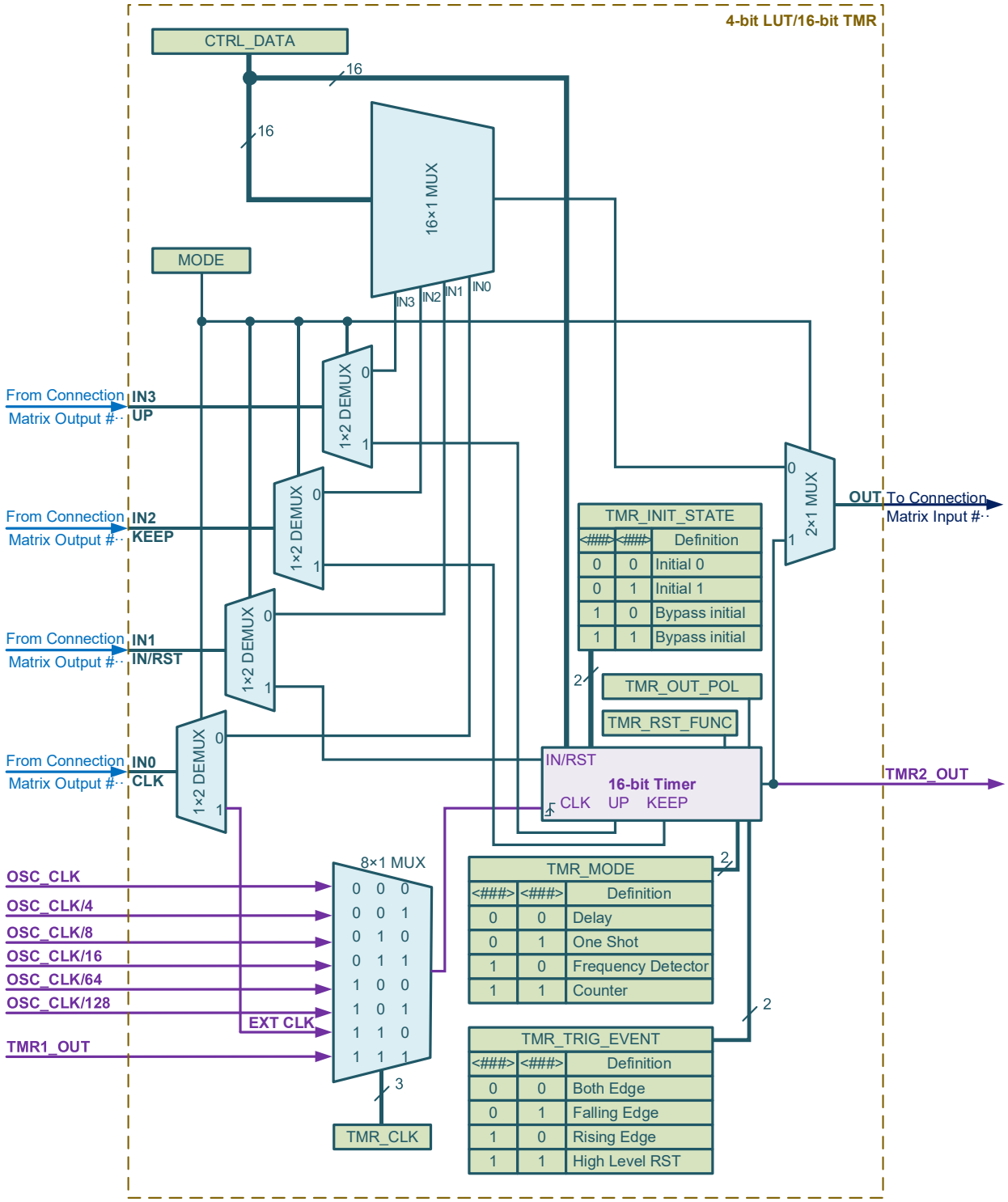


Figure 8.7. 4-bit LUT0/TMR2

8.5.1. MF8 (4-bit LUT0/TMR2)

Settings of MF8 (4-bit LUT0/TMR2) is set out in Table 8.24.

Table 8.24. MF8 (4-bit LUT0/TMR2) Register Settings

Register Bit Address	Register Name	Register Definition
MF8 (3-bit LUT9/8-bit TMR1)		
<314:299>	MF8_CTRL_DATA	MF control data
<316:315>	MF8_TMR_MODE	Timer mode: 00: Delay 01: One shot 10: Frequency detector 11: Counter
<319:317>	MF8_TMR_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR1_OUT
<321:320>	MF8_TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<322>	MF8_TMR_RST_FUNC	Reset functionality: 0: Reset to 0 1: Set to Control data
<323>	MF8_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<324>	MF8_MODE	MF mode: 0: LUT 1: Timer
<488:487>	MF8_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial

The MF8 (4-bit LUT0/TMR2) macrocell, if programmed for a LUT function, uses 16-bit register to define its output function by reg<314:299> (see Table 8.12).

Table 8.25. MF8 (4-bit LUT0) Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	MF8_CTRL_DATAL<0>	LSB
0	0	0	1	MF8_CTRL_DATAL<1>	
0	0	1	0	MF8_CTRL_DATAL<2>	
0	0	1	1	MF8_CTRL_DATAL<3>	
0	1	0	0	MF8_CTRL_DATAL<4>	
0	1	0	1	MF8_CTRL_DATAL<5>	
0	1	1	0	MF8_CTRL_DATAL<6>	
0	1	1	1	MF8_CTRL_DATAL<7>	
1	0	0	0	MF8_CTRL_DATAL<8>	
1	0	0	1	MF8_CTRL_DATAL<9>	
1	0	1	0	MF8_CTRL_DATAL<10>	
1	0	1	1	MF8_CTRL_DATAL<11>	
1	1	0	0	MF8_CTRL_DATAL<12>	
1	1	0	1	MF8_CTRL_DATAL<13>	
1	1	1	0	MF8_CTRL_DATAL<14>	
1	1	1	1	MF8_CTRL_DATAL<15>	MSB

9. Timers (TMR)

The AM1U1108 has three configurable 8-bit timers (TMR0, TMR1 – see Figure 9.36, TMR3 – see Figure 9.37).

TMR0 and TMR1 have one input from the connection matrix for IN/RST, and one for an external counter/clock source (for a total of two inputs from the connection matrix). One of the Timer macrocells (TMR3) has one input from the connection matrix which has a shared function of IN or external CLK input. The outputs of TMR0 and TMR1 go back to the conncection matrix. TMR3 has an additional output of Edge Detector.

Each timer has the following mode of operation:

- Delay
- Counter
- One Shot
- Frequency Detector
- Delayed Edge Detector
- Edge Detector

The output polarity of the TMR is configurable and can be selected as non-inverted or inverted.

In the Delay mode the TMR delays the input signal by the selected edge event (rising edge, falling edge, both edges) for a time determined by the Control Data, input clock signal and selected divider value. If input signal is shorter than the delay value, the signal does not propagate to the output. The timing diagrams of this mode is shown in the Figure 9.1…Figure 9.6.

In the Counter mode the TMR divides input clock signal by the value determined by the Control Data, input clock signal and selected divider value. The output of the TMR goes HIGH every time when the Counted Value (current value of the counter) is equal 0. The RST in of the TMR reset Counted value to 0 by one of the following events: rising edge, falling edge, both edges, high level. The timing diagrams of this mode is shown in the Figure 9.7…Figure 9.12.

In One-Shot mode this macrocell generates a high-level pulse with a set width, when detecting the edge event, which is selectable by the registers, on its IN input. The pulse width is determined by the Control Data, input clock signal and selected divider value. Any incoming edges are ignored during pulse width generation. The timing diagrams of this mode is shown in the Figure 9.13…Figure 9.18.

In Frequency Detector mode the TMR function following scenarios:

- Rising Edge: The output will go HIGH if the time between two rising edges is less than the delay.
  The output will go LOW if the next rising edge has not come after the last rising edge in specified time.
- Falling Edge: The output will go HIGH if the time between two falling edges is less than the set time.
  The output will go LOW if the next falling edge has not come after the last falling edge in specified time.
- Both Edges: The output will go HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse.
  The output will go LOW if the next rising/falling edge has not come after the last falling/rising edge in specified time.

The timing diagrams of the Frequency Detector Mode is shown in the Figure 9.19…Figure 9.24.

In the Delayed Edge Detector mode the TMR generates delayed short high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The delay time is determined by the Control Data, input clock signal and selected divider value. The timing diagrams of this mode is shown in the Figure 9.25…Figure 9.30.

In Edge Detector mode the TMR generates short high level pulse (for non-inverted polarity) when detecting the respective selected edge event (rising edge, falling edge, both edges). The timing diagrams of this mode is shown in the Figure 9.31.

Time of Timers for each mode can be calculated using the following formulas (Note 8.9, Note 8.10):

- Delay (Figure 9.1…Figure 9.6)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK};
- Counter Figure 9.7…Figure 9.12)
  Output Period = (Control Data + 1)/F_{CLK};
  Output Frequency = F_{CLK}/(Control Data + 1);
- One Shot (Figure 9.13…Figure 9.18)
  Pulse width = (Control Data + 1 + VAR)/F_{CLK};
- Frequency Detector (Figure 9.19…Figure 9.24)
  Detected Frequency = F_{CLK}/(Control Data + 1 + VAR).
- Delayed Edge Detector (Figure 9.25…Figure 9.30)
  Delay Time = (Control Data + 1 + VAR)/F_{CLK}.

Note 9.1 *F_{CLK} – CLK input frequency.*

Note 9.2 *VAR = 0…1 – defined by the asynchronous time between the input signal and the first clock pulse.*

Note 9.3 *Counters initialize with Control Data after POR.*

There is also one Multifunctional Macrocells that can implement either 4-bit LUT or 16-bit TMR (See Section 8.5 MF (4-bit LUT0/16-Bit Timer) Macrocells).

9.1. TMR Timing Diagrams

9.1.1. Delay Mode (Control Data: 4)

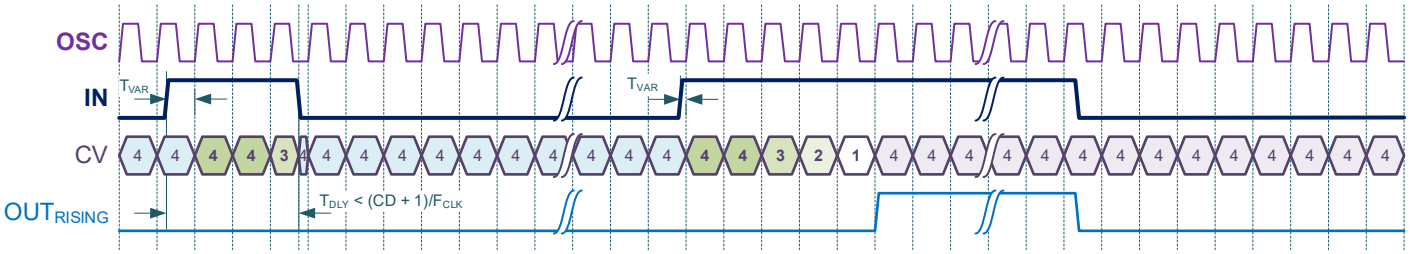


Figure 9.1. Delay Mode Timing Diagram (Rising Edge Detect, Forced OSC)

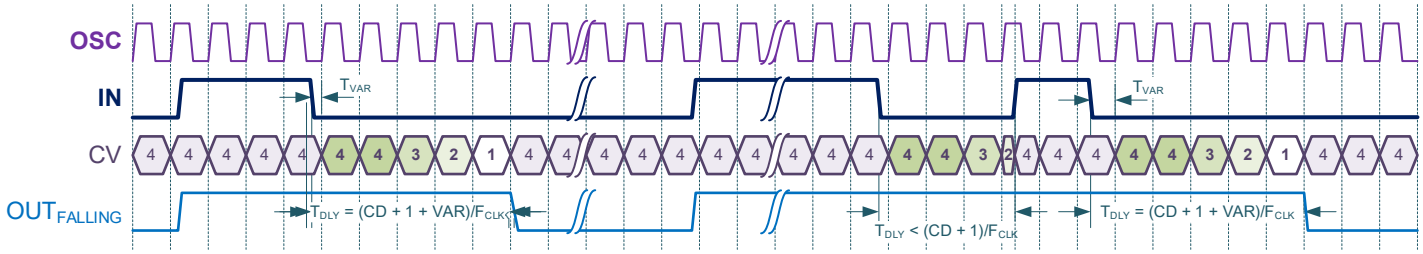


Figure 9.2. Delay Mode Timing Diagram (Falling Edge Detect, Forced OSC)

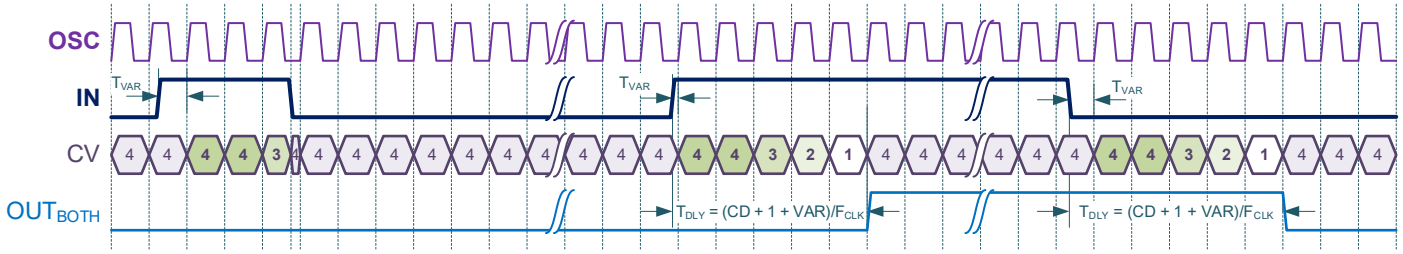


Figure 9.3. Delay Mode Timing Diagram (Both Edge Detect, Forced OSC)

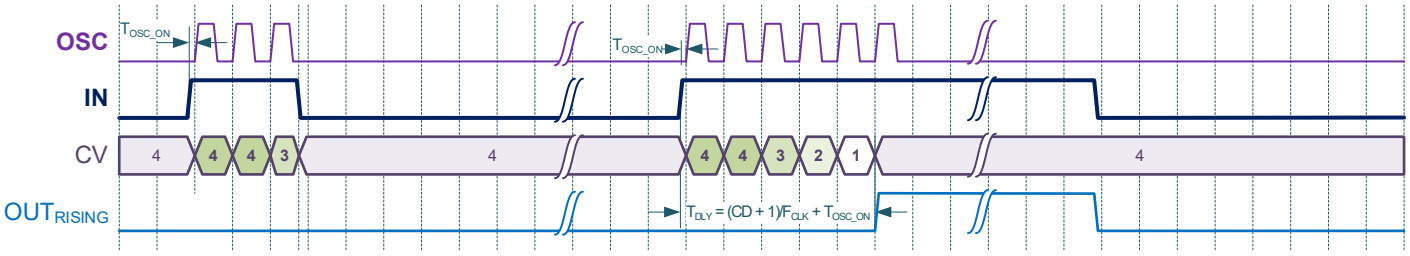


Figure 9.4. Delay Mode Timing Diagram (Rising Edge Detect, Auto OSC)

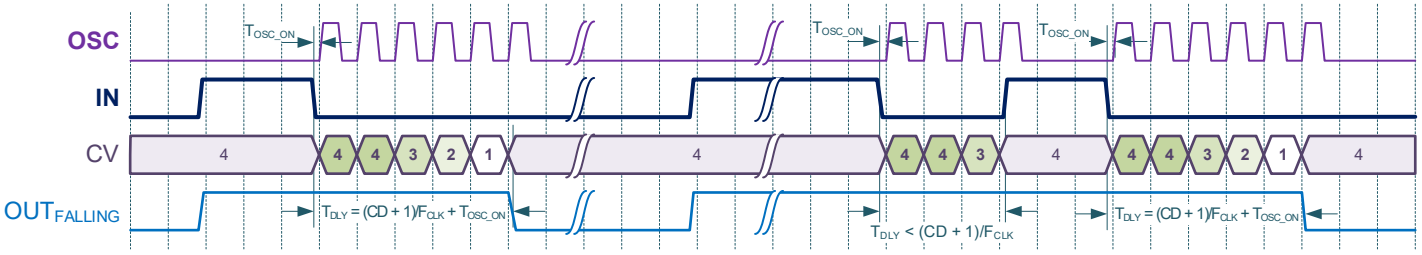


Figure 9.5. Delay Mode Timing Diagram (Falling Edge Detect, Auto OSC)

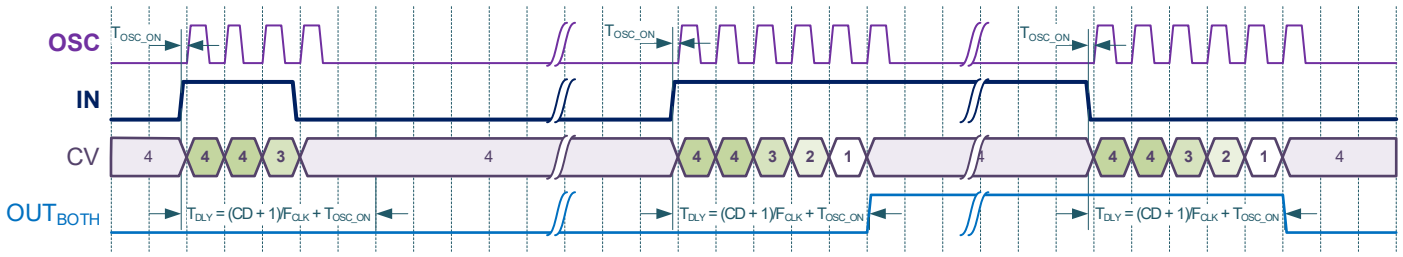


Figure 9.6. Delay Mode Timing Diagram (Both Edge Detect, Auto OSC)

9.1.2. Counter Mode (Control Data: 4)

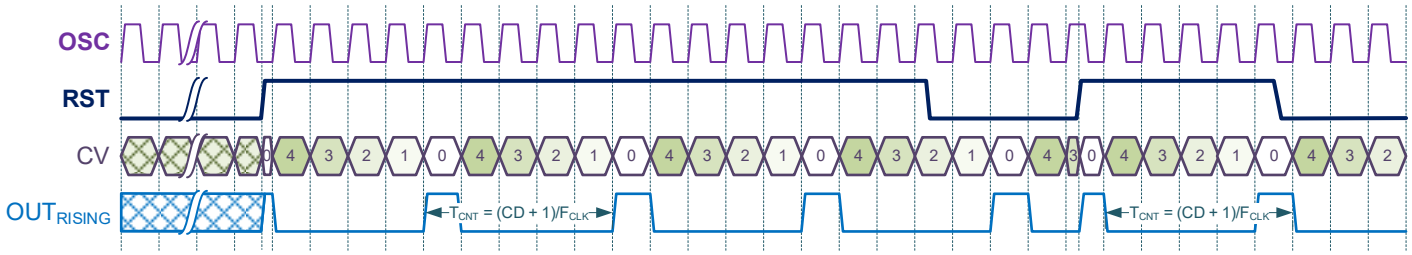


Figure 9.7. Counter Mode Timing Diagram (TMR0, TMR1, Rising Reset, Forced OSC, Auto OSC)

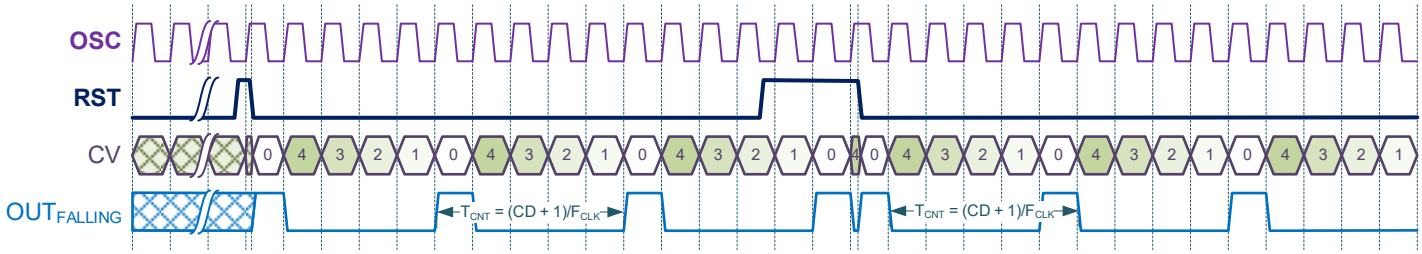


Figure 9.8. Counter Mode Timing Diagram (TMR0, TMR1, Falling Reset, Forced OSC, Auto OSC)

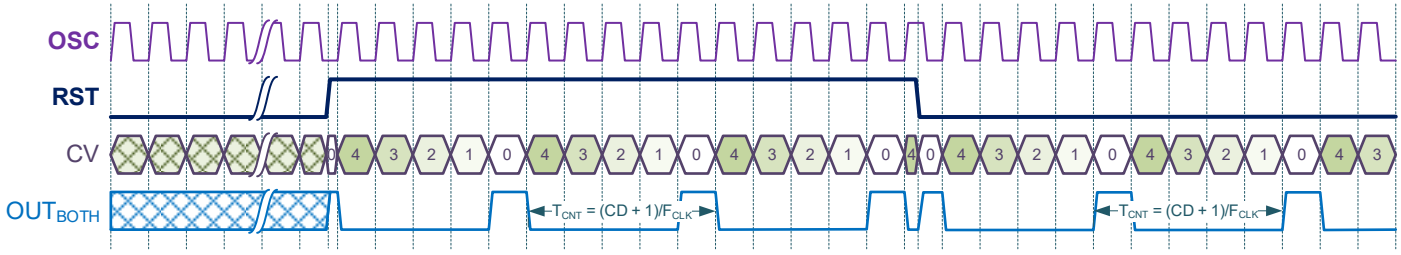


Figure 9.9. Counter Mode Timing Diagram (TMR0, TMR1, Both Edge Reset, Forced OSC, Auto OSC)

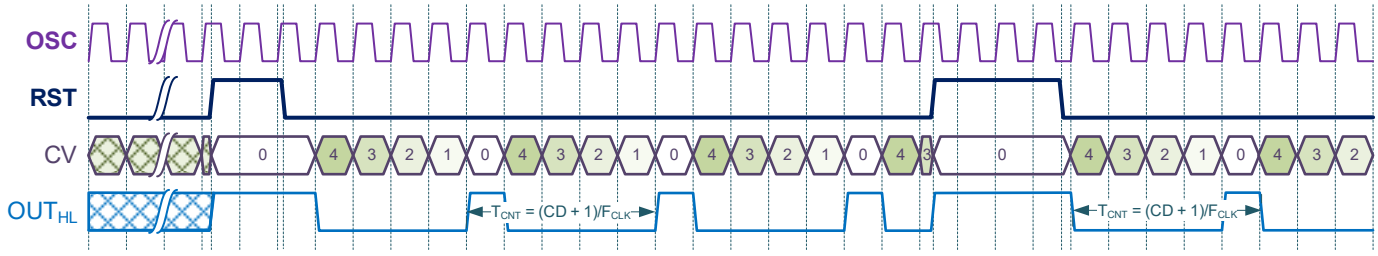


Figure 9.10. Counter Mode Timing Diagram (TMR0, TMR1, High Level Reset, Forced OSC)

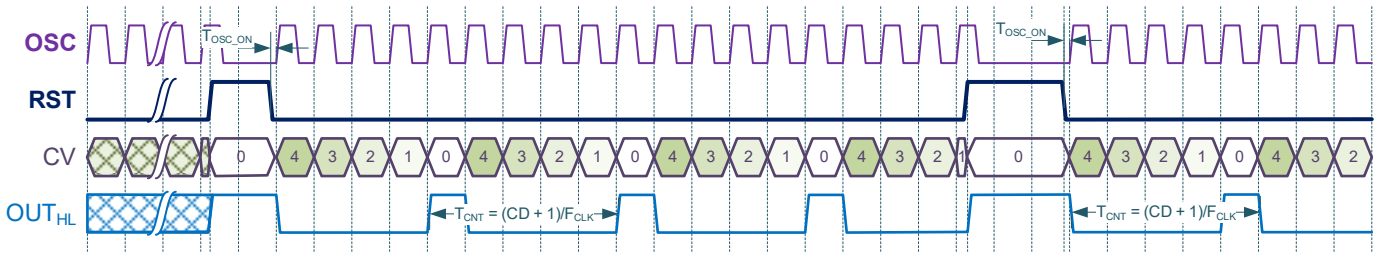


Figure 9.11. Counter Mode Timing Diagram (TMR0, TMR1, High Level Reset, Auto OSC)

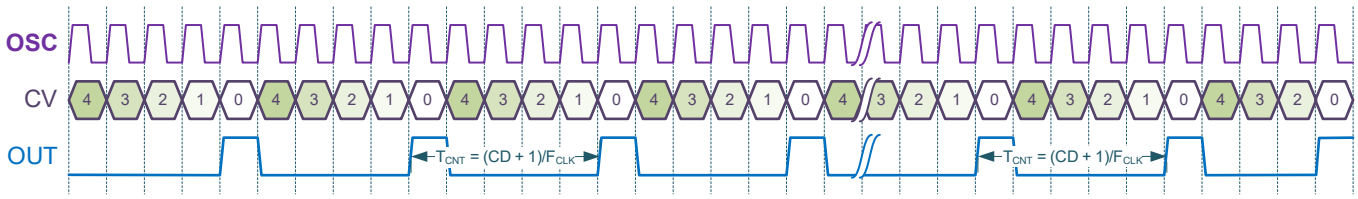


Figure 9.12. Counter Mode Timing Diagram (TMR3, Auto OSC, Forced OSC)

9.1.3. One-Shot Generator Mode (Control Data: 4)

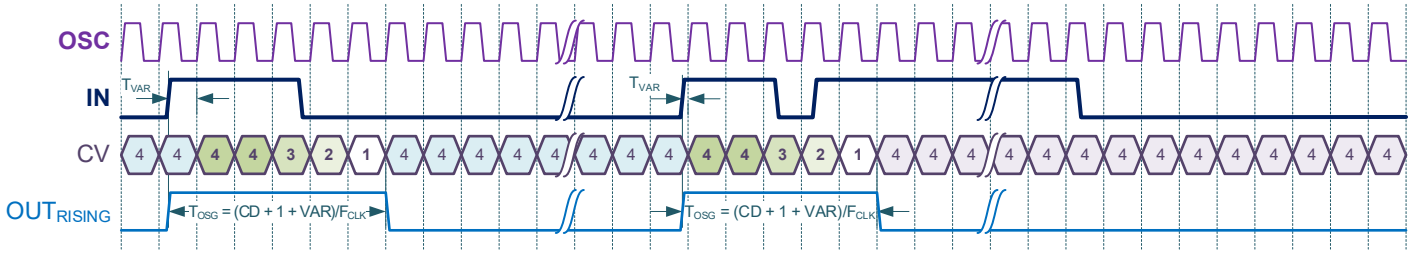


Figure 9.13. One-Shot Generator Mode Timing Diagram (Rising Edge, Forced OSC)

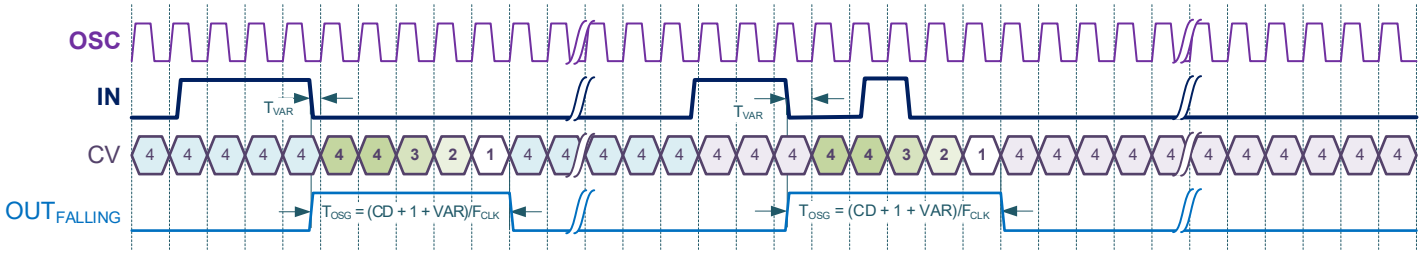


Figure 9.14. One-Shot Generator Mode Timing Diagram (Falling Edge, Forced OSC)

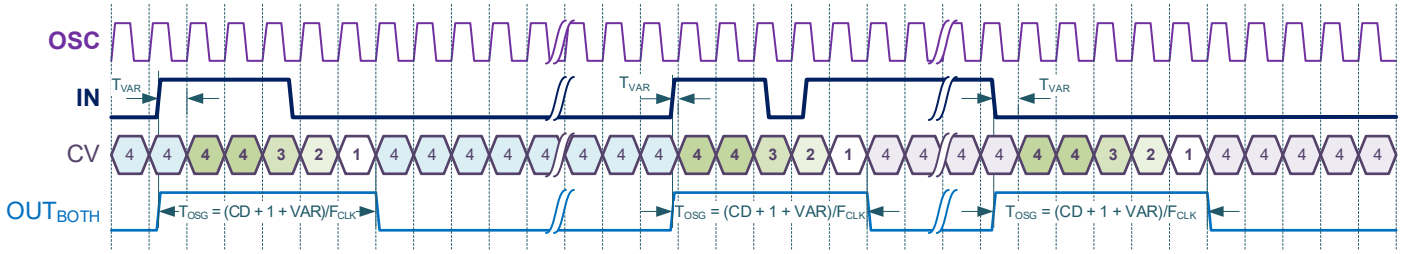


Figure 9.15. One-Shot Generator Mode Timing Diagram (Both Edge, Forced OSC)

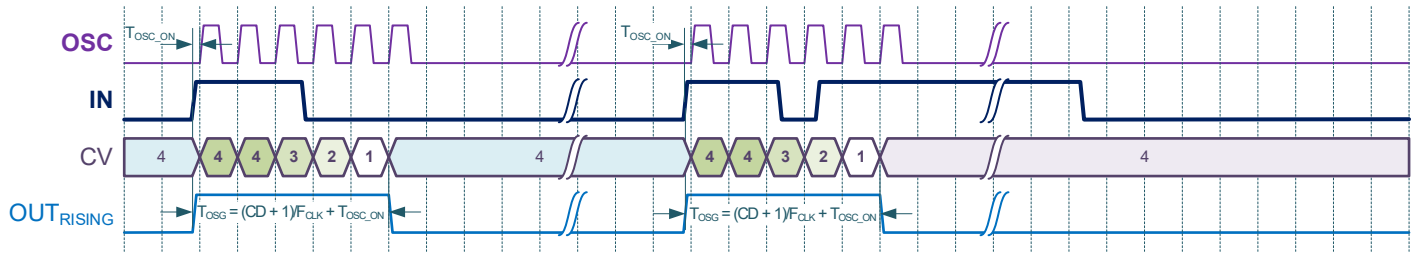


Figure 9.16. One-Shot Generator Mode Timing Diagram (Rising Edge, Auto OSC)

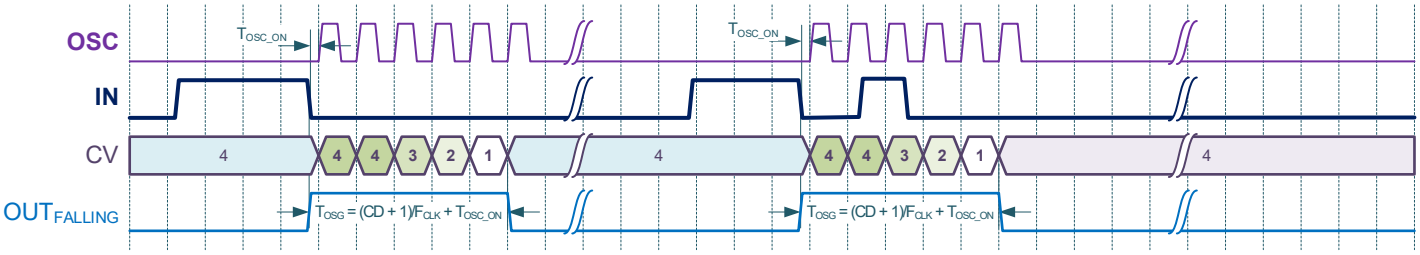


Figure 9.17. One-Shot Generator Mode Timing Diagram (Falling Edge, Auto OSC)

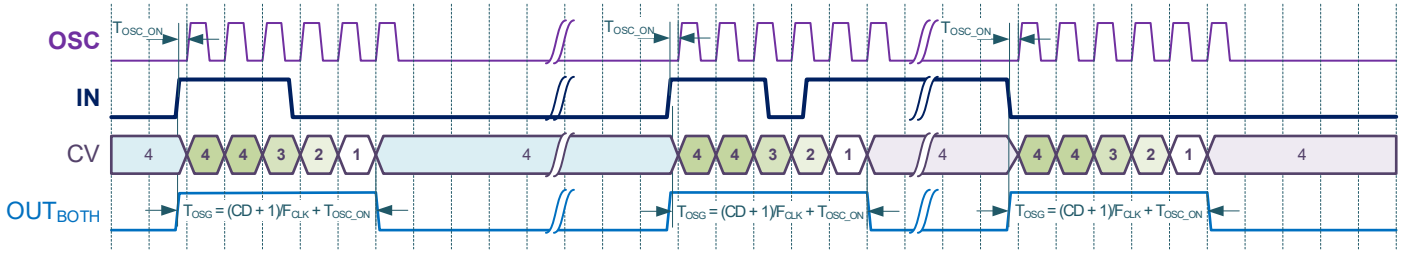


Figure 9.18. One-Shot Generator Mode Timing Diagram (Both Edge, Auto OSC)

9.1.4. Frequency Detector Mode (Control Data: 4)

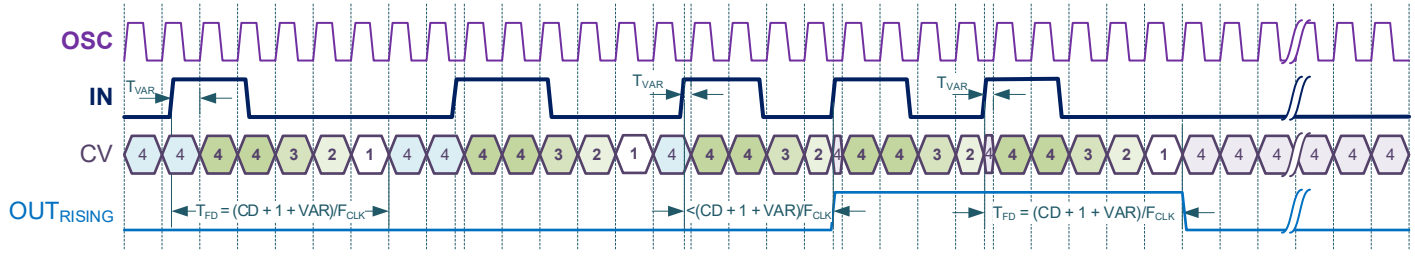


Figure 9.19. Frequency Detector Mode Timing Diagram (Rising Edge, Forced OSC)

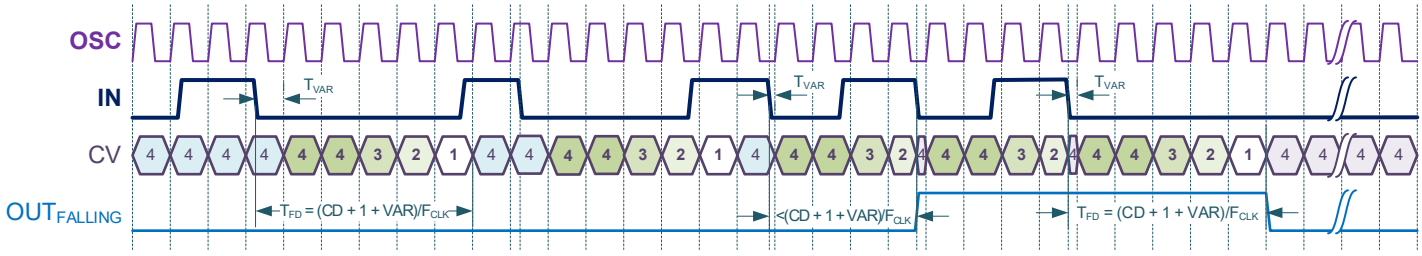


Figure 9.20. Frequency Detector Mode Timing Diagram (Falling Edge, Forced OSC)

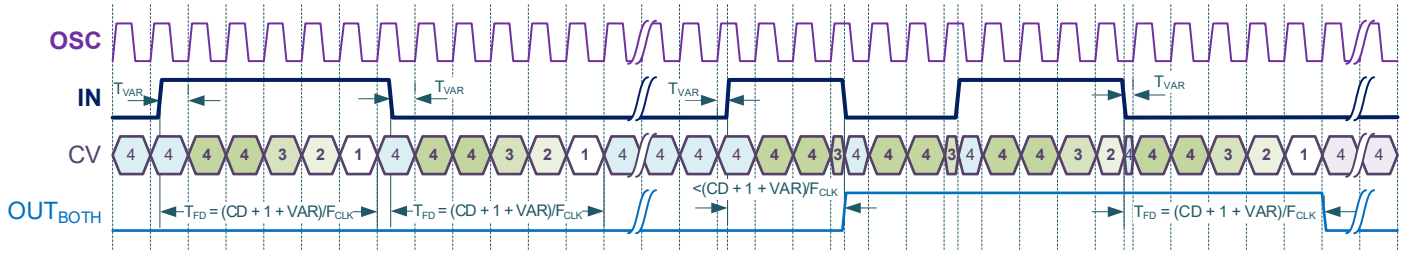


Figure 9.21. Frequency Detector Mode Timing Diagram (Both Edge, Forced OSC)

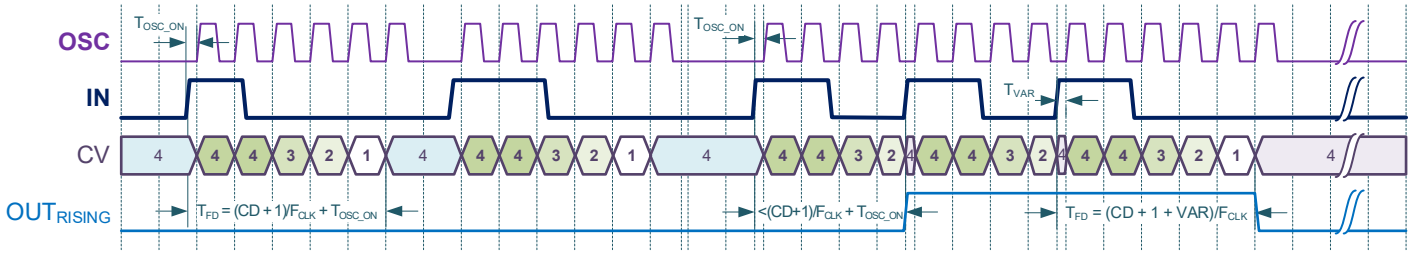


Figure 9.22. Frequency Detector Mode Timing Diagram (Rising Edge, Auto OSC)

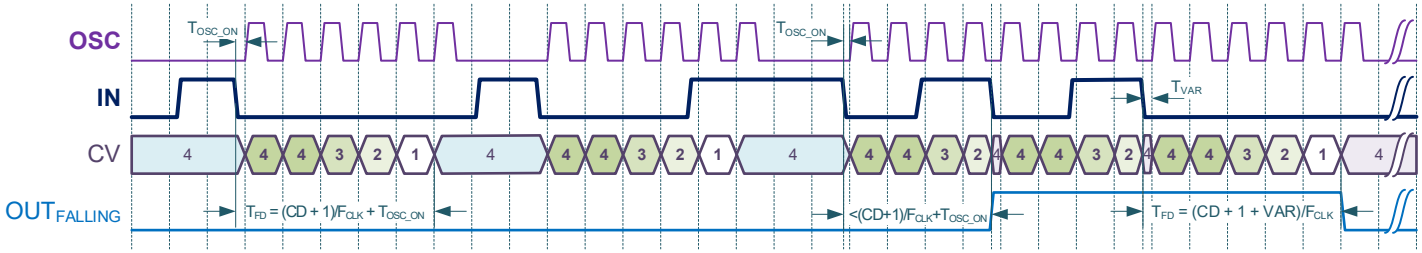


Figure 9.23. Frequency Detector Mode Timing Diagram (Falling Edge, Auto OSC)

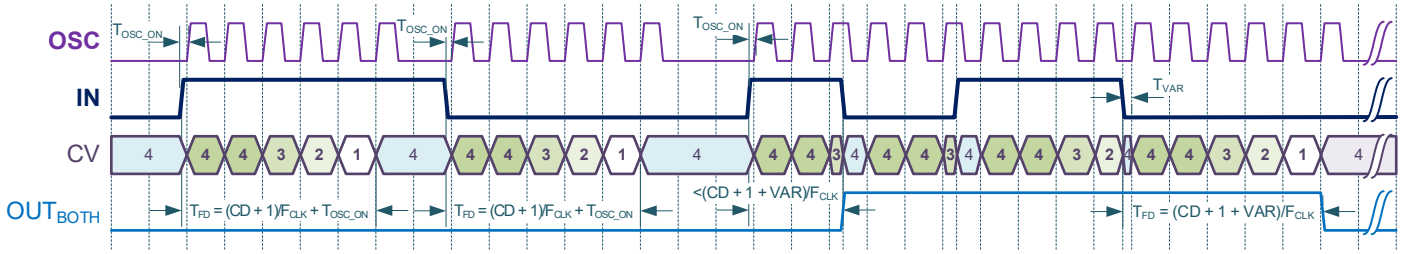


Figure 9.24. Frequency Detector Mode Timing Diagram (Both Edge, Auto OSC)

9.1.5. Delayed Edge Detector Mode TMR0, TMR1

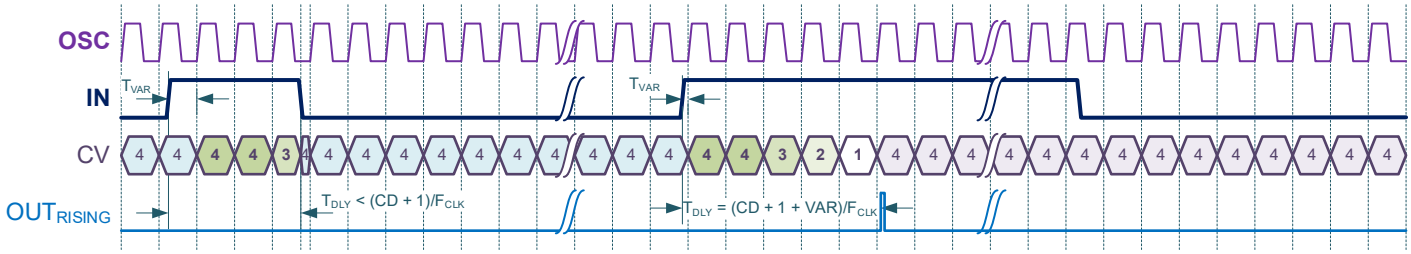


Figure 9.25. Delay Edge Detector Mode Timing Diagram (Rising Edge, Forced OSC)

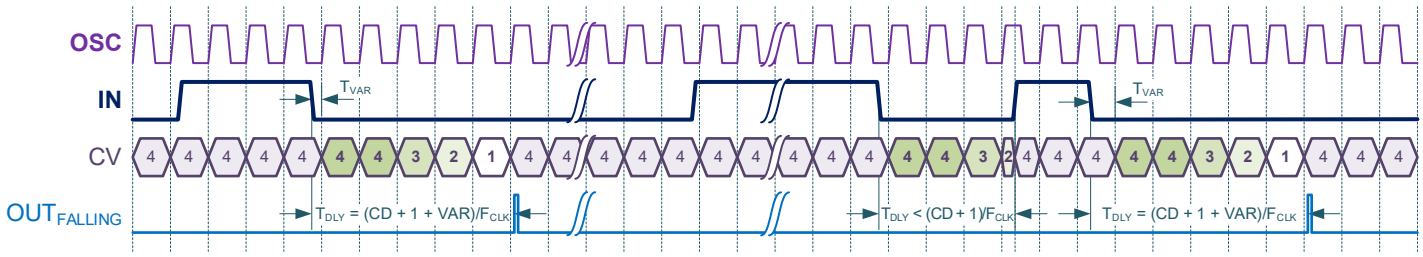


Figure 9.26. Delay Edge Detector Mode Timing Diagram (Falling Edge, Forced OSC)

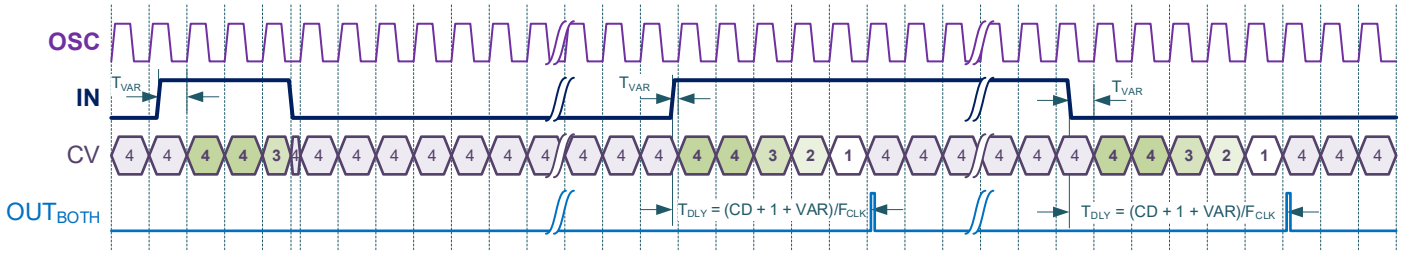


Figure 9.27. Delay Edge Detector Mode Timing Diagram (Both Edge, Forced OSC)

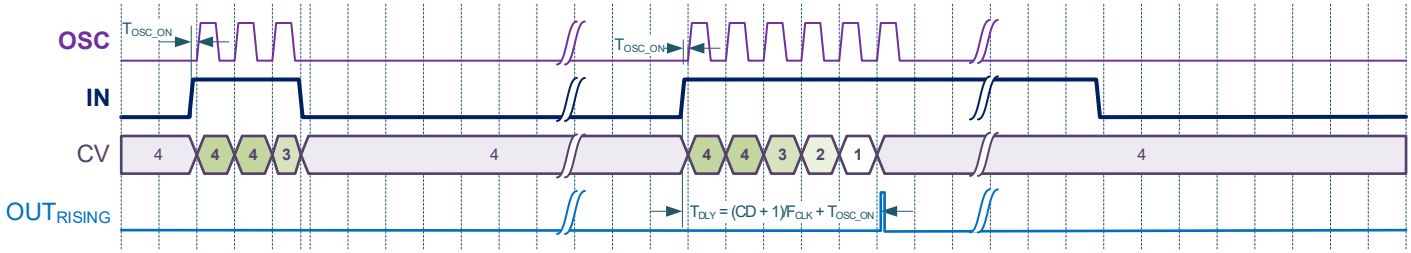


Figure 9.28. Delay Edge Detector Mode Timing Diagram (Rising Edge, Auto OSC)

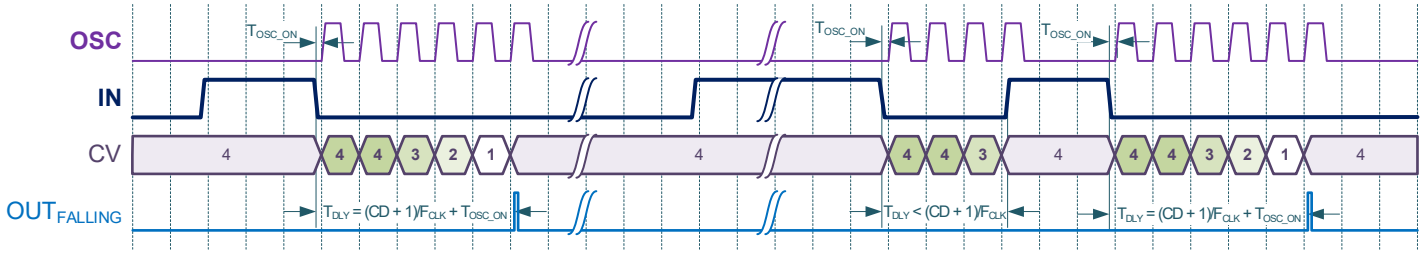


Figure 9.29. Delay Edge Detector Mode Timing Diagram (Falling Edge, Auto OSC)

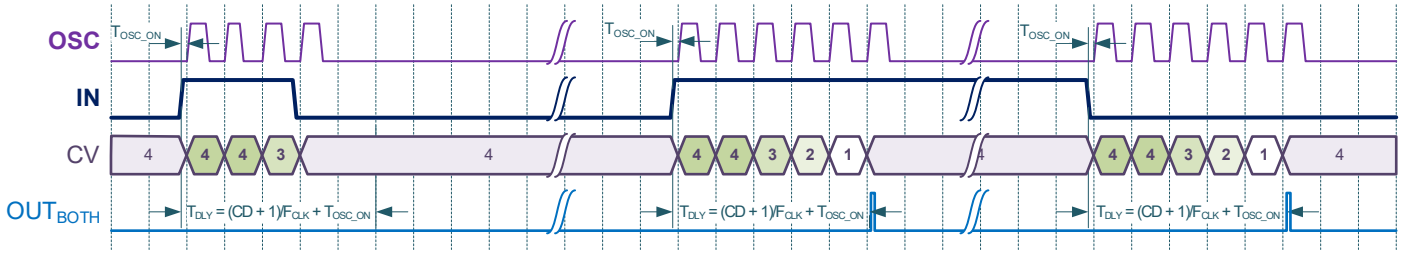


Figure 9.30. Delay Edge Detector Mode Timing Diagram (Both Edge, Auto OSC)

9.1.6. Edge Detector Mode TMR0, TMR1, TMR3 (EDGE out)

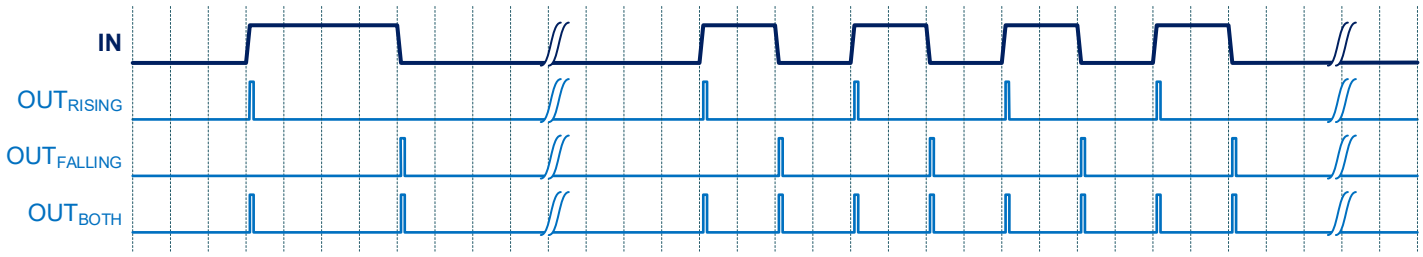


Figure 9.31. Edge Detector Mode Timing Diagram

9.1.7. Counter Mode TMR2 (Control Data: 4)

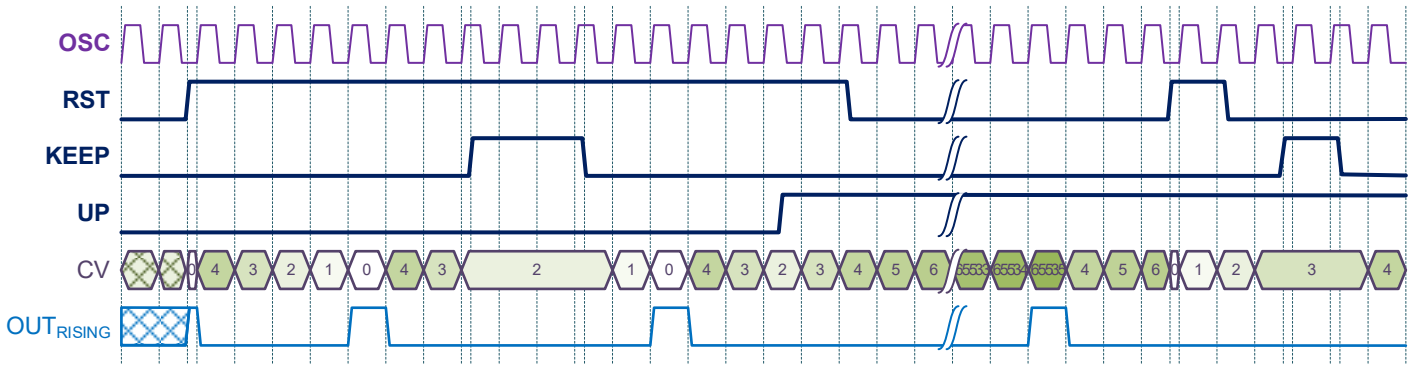


Figure 9.32. TMR2 Counter Mode Timing Diagram (Rising Reset, Forced OSC)

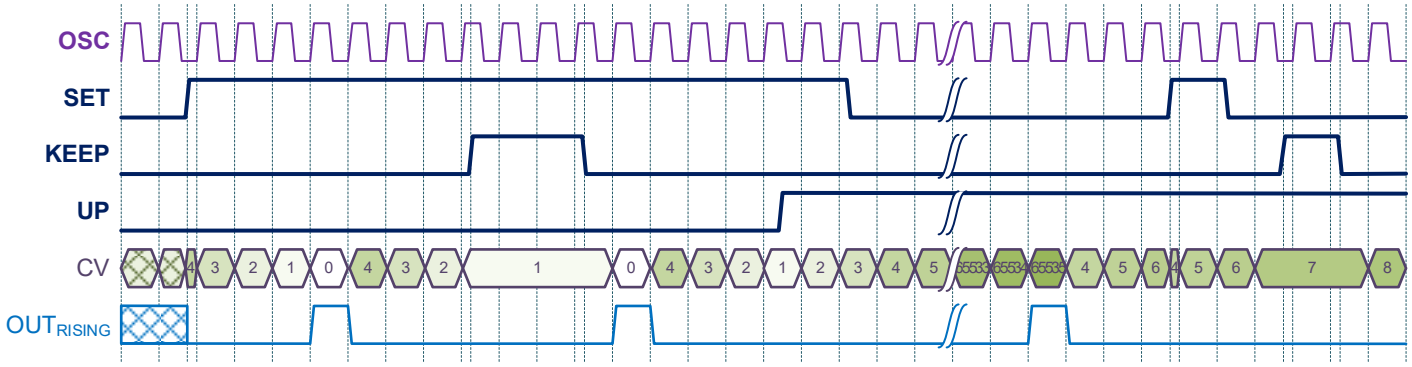


Figure 9.33. TMR2 Counter Mode Timing Diagram (Rising Set, Forced OSC)

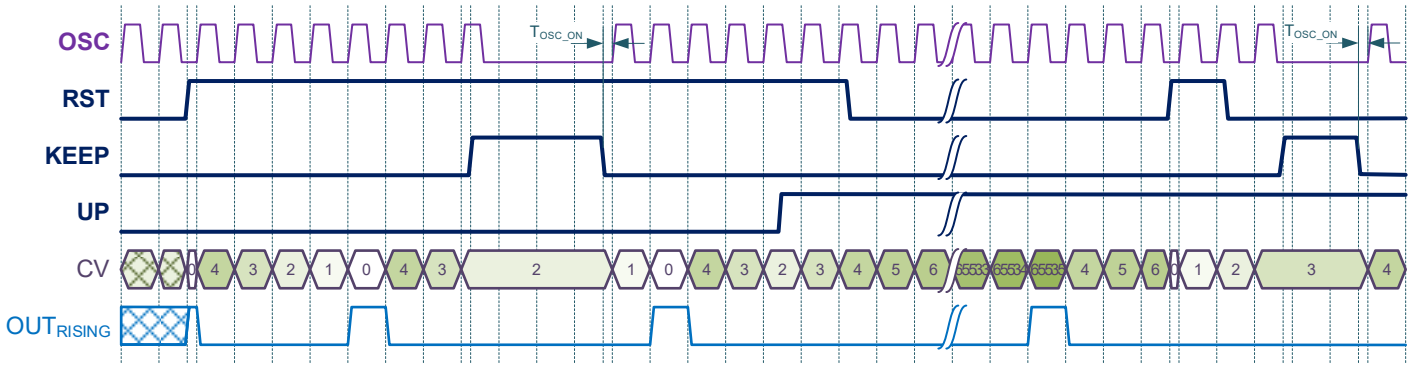


Figure 9.34. TMR2 Counter Mode Timing Diagram (Rising Reset, Auto OSC)

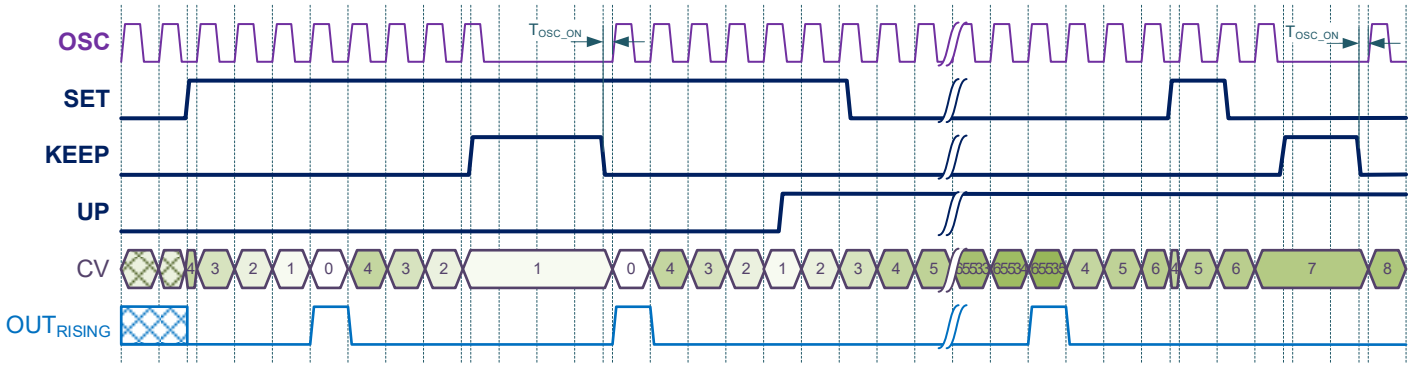


Figure 9.35. TMR2 Counter Mode Timing Diagram (Rising Set, Auto OSC)

9.2. 8-bit TMR0

Schematic diagram of TMR0 macrocell is shown in Figure 9.36. Its register settings set out in Table 9.1.

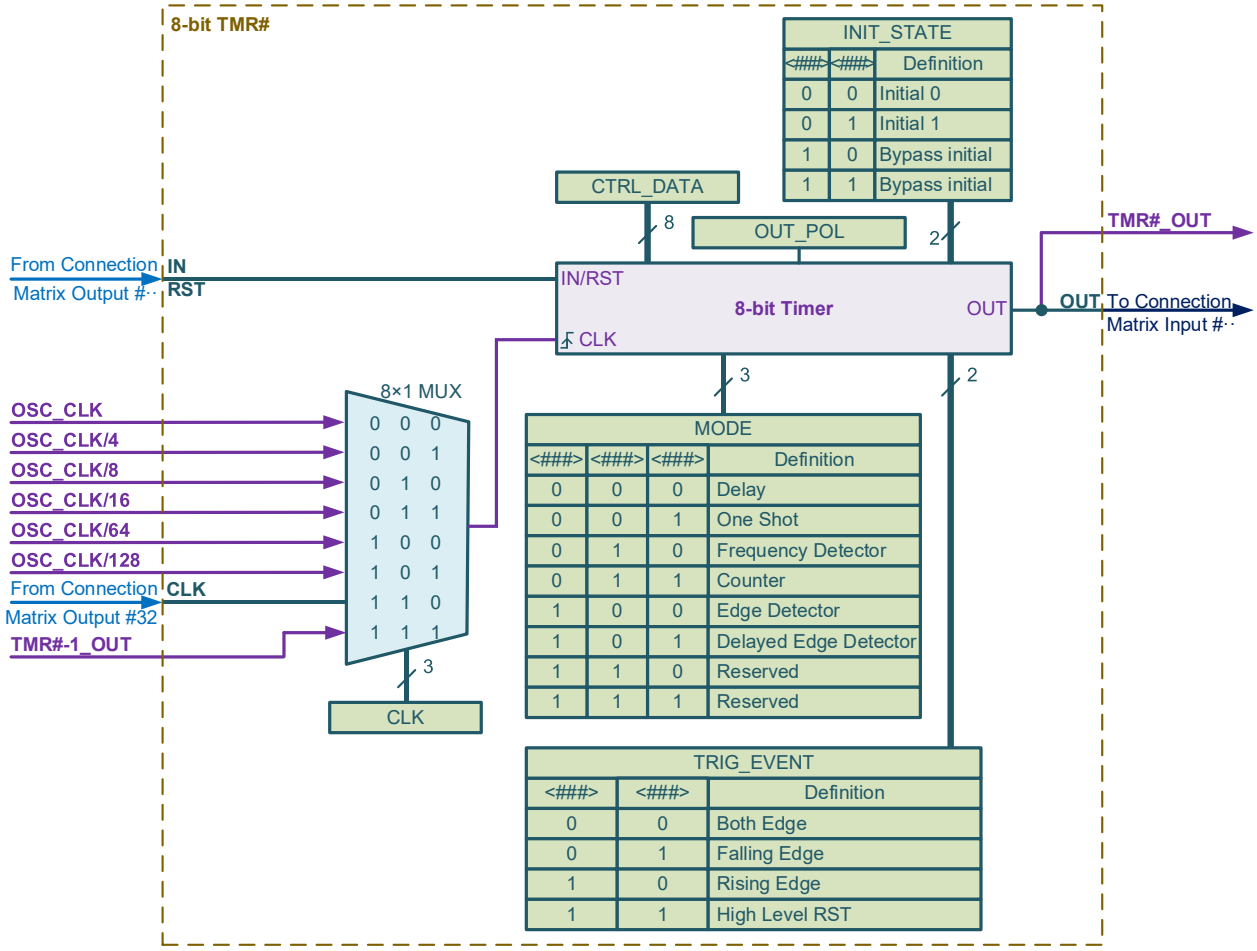


Figure 9.36. TMR0, TMR1

Table 9.1. TMR0 Register Settings

Register Bit Address	Register Name	Register Definition
8-bit TMR0		
<350:343>	TMR0_CTRL_DATA	Timer control data
<352:351>	TMR0_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<355:353>	TMR0_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR3_OUT
<358:356>	TMR0_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<359>	TMR0_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<472:471>	TMR0_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial

9.3. 8-bit TMR1

Schematic diagram of TMR1 macrocell is shown in Figure 9.36. Its register settings set out in Table 9.2.

Table 9.2. TMR1 Register Settings

Register Bit Address	Register Name	Register Definition
8-bit TMR1		
<367:360>	TMR1_CTRL_DATA	Timer control data
<379:378>	TMR1_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<382:380>	TMR1_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR0_OUT
<385:383>	TMR1_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<386>	TMR1_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<474:473>	TMR1_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial

9.4. 8-bit TMR3

Schematic diagram of TMR3 macrocell is shown on Figure 9.37. Its register settings set out in Table 9.3.

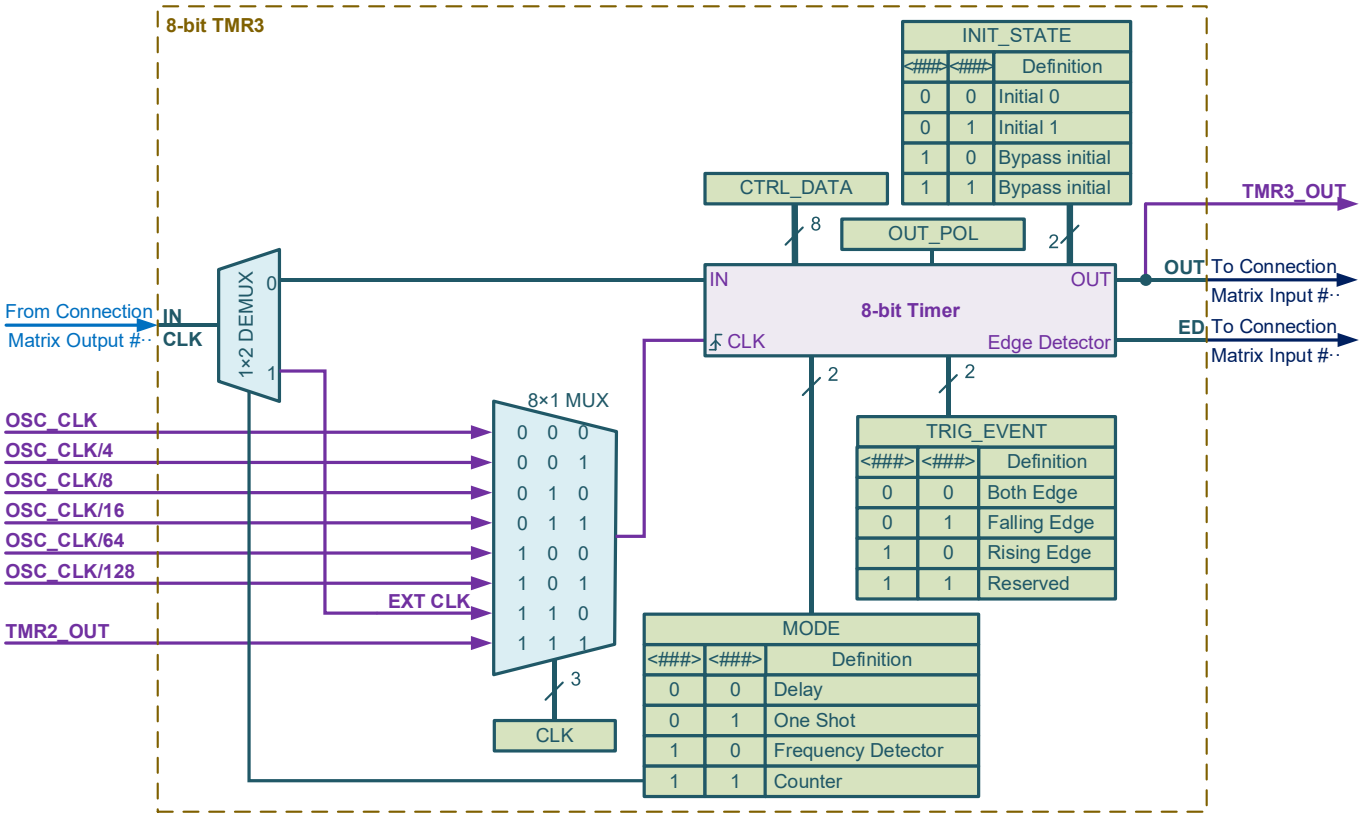


Figure 9.37. TMR3

Table 9.3. TMR3 Register Settings

Register Bit Address	Register Name	Register Definition
8-bit TMR3		
<395:388>	TMR3_CTRL_DATA	Timer control data
<397:396>	TMR3_MODE	Timer mode: 00: Delay 01: One shot 10: Frequency detector 11: Counter
<400:398>	TMR3_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR0_OUT
<402:401>	TMR3_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: Reserved
<403>	TMR3_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<496:495>	TMR3_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial

10. Memory Architecture

The Memory of µASIC consists of two main parts: non-volatile memory (NVM) and registers. The configuration of the µASIC is stored in the NVM and is loaded to the volatile registers, during device power on. The registers values define macrocells configuration, matrix connections setting (signal routing), IO configuration etc., that allows to get the desired functionality for user's application (see Figure 10.1).

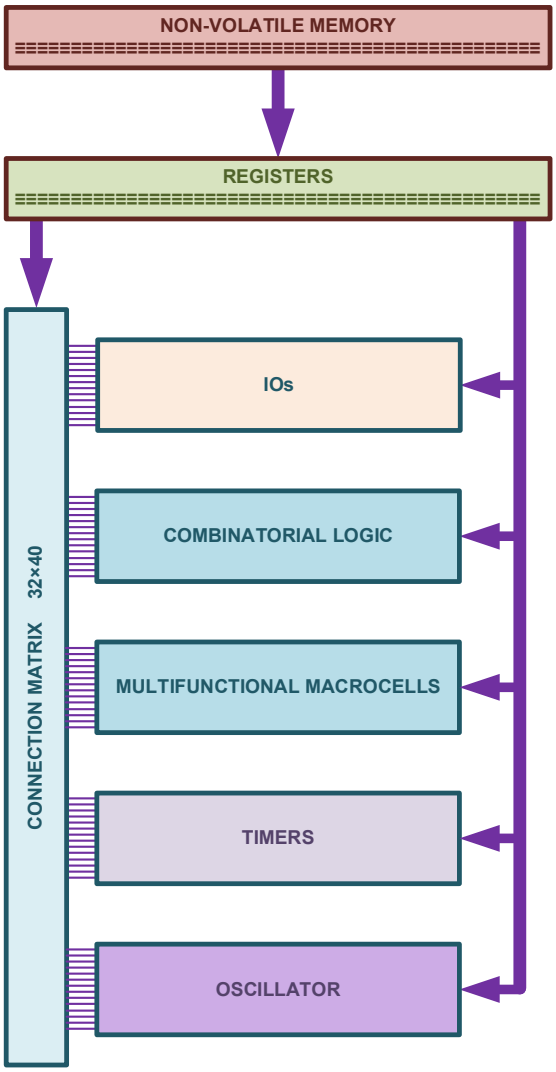


Figure 10.1. Memory Architecture

11. Data Protection

The AM1U1108 has data protection that is provided by CRV.

Table 11.1. Security Control Registers

Register Bit Address	Register Name	Register Definition
Security Control		
<456>	SYS_SECURITY_CRV_EN	Continuous register verification: 0: Disable 1: Enable

Continuous Registers Verification (CRV) is provided by a continuous comparison the register bits <501, 411, 377, 376, 368, 342, 327, 219, 191, 140, 84, 43, 42, 41, 15> with hardcoded value 15'b011001100001101. If the comparison shows a mismatch the AM1U1108 automatically restarts.

12. Oscillator (OSC)

AM1U1108 has an internal Oscillators with two selectable frequencies: 25 kHz and 2 MHz. OSC macrocell can be sourced from internal oscillator or by external frequency from IO8.

The OSC has two prescaler stages that gives user flexibility for introducing clock signals on the Connection Matrix Input lines. The first stage ($CLK_{Prescale}$) allows to divide the fundamental frequency by **/1**, **/2**, **/4** or **/8**. The two independent second stage prescaler allow to divide the frequency from the first stage divider by **/1**, **/4**, **/8**, **/16, /32, /64** or **/128**, and outputs this frequency on the Connection Matrix Input #21 and #22 (See Figure 12.1 for more details).

When internal OSC is used, there is a choice between “Force Power On”, meaning that the OSC will always run, or “Auto Power On”, meaning that the OSC will run only on demand of internal logics (TMRs) and consequently have an associated startup and settling time.

The oscillator is turned on when the PWRDWN signal is LOW and turned off when the PWRDWN signal is HIGH. The PWRDWN signal has the highest priority.

Schematic diagram of the OSC macrocell is shown in Figure 12.1. Its register settings set out in Table 12.3.

AM1U1108 has an internal oscillator that allows to cover a variety of application:

- OSC with two selectable output frequencies 25 kHz or 2 MHz.

OSC macrocell can be sourced either from internal oscillator or by external frequency from IO8.

The OSC has two divider stages that gives user flexibility for introducing clock signals on the Connection Matrix Input lines. The first stage (prescaler) allows to divide the fundamental frequency by **/1**, **/2**, **/4** or **/8**. The two independent second stage dividers allow to divide the frequency from the first stage divider by **/1**, **/2, /4**, **/8**, **/16, /32, /64, /128** and outputs this frequency on the Connection Matrix Input #21 and #22 (See Figure 12.1 and Table 12.3 for more details).

Each oscillator has three power states of operation (see Table 12.1). The flow of turning on the oscillator is started from OFF state, then it goes to IDLE state and last is ON state in which frequency appear on the oscillator output.

Table 12.1. Oscillator power states

State	Description
OFF state	The oscillator is fully shut down and consumes the minimum amount of current (less than 1nA). The power on time of the oscillator is longer compare to the power on from the IDLE state (see Table 4.10, Table 4.14). The oscillator stays in this state when it is not turned on by timers or control input, and Power On Time is selected as normal.
IDLE state	The power consumption is higher compared to the OFF state and depends on the type of oscillator (see Table 4.5). The oscillator is ready to operate and power on time is within 1 clock cycle of the oscillator.
ON state	The oscillator consumes its active current and frequency is generated on the oscillator output (see Table 4.5)

Each oscillators have three settings that allow to choose appropriate mode of operation (see Table 12.2).

Table 12.2. Oscillator setting

Setting	Option	Description
Power On Time	Normal	The oscillator power on time is normal (see Table 4.10, Table 4.14). When the oscillator is turned off it stays in the OFF state.
	Fast	The oscillator power on time fast, within 1 clock cycle (see Table 4.10, Table 4.14). When the oscillator is turned off it stays in the IDLE state.
Power Mode	Auto power on	The oscillator is turned on when any of timers require it (Note 12.1).
	Forced power on	The oscillator is turned on when part is powered on and PWR_DWN signal doesn’t shut down it.

Note 12.1 PWR_DWN signal has the highest priority and sut down the oscillator.

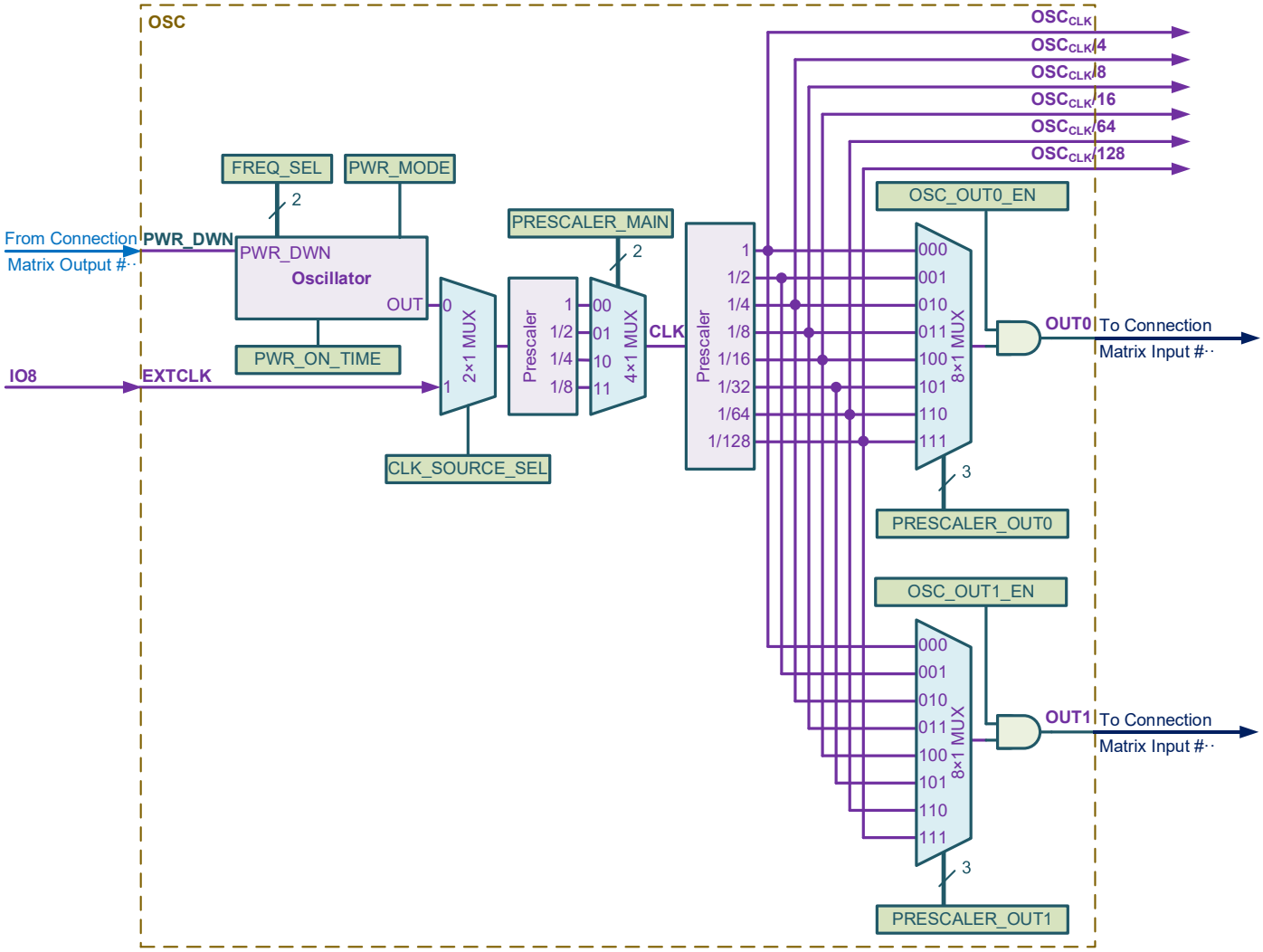


Figure 12.1. OSC Block Diagram

Table 12.3. OSC Register Settings

Register Bit Address	Register Name	Register Definition
OSC (25kHz/2MHz)		
<225:224>	OSC_FREQ_SEL	Frequency: 00: Both disable 01: 25kHz 10: 2MHz 11: Both enable
<325>	OSC_PWR_MODE	Power mode: 0: Auto power on 1: Forced power on
<326>	OSC_PWR_ON_TIME	Power on time: 0: Normal 1: Fast
<336>	OSC_CLK_SOURCE_SEL	Clock source: 0: Inner oscillator 1: External CLK
<329:328>	OSC_PRESCALER_MAIN	Main prescaler: 00: 1 01: 1/2 10: 1/4 11: 1/8
<332:330>	OSC_PRESCALER_OUT0	OUT0 prescaler: 000: OUT0_DISABLE 001: OSC_CLK 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<335:333>	OSC_PRESCALER_OUT1	OUT1 prescaler: 000: OUT1_DISABLE 001: OSC_CLK/2 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<374>	OSC_OUT0_EN	OUT0 enable: 0: OUT0 disable 1: OUT0 enable
<375>	OSC_OUT1_EN	OUT1 enable: 0: OUT1 disable 1: OUT1 enable

13. Power On Reset (POR)

To ensure correct device initialization and operation of all macrocells in the device, the µASIC has a Power-On Reset (POR) circuit. The POR circuit achieves consistent behavior and predictable results during VDD power ramp up and power down. To accomplish this goal, the POR circuit releases a defined Power-Up sequence of internal events that initialize different macrocells inside the device.

13.1. POR General Operation

To start the Power-Up sequence, the voltage applied on the VDD should be higher than the POWER ON threshold (which can vary by PVT, but typical is 1.6 V). The operational V_{DD} range for the AM1U1108 is 1.71V…5.50V. Therefore, the Power-Up sequence will start earlier, as soon as the V_{DD} rises to the POWER ON threshold, but the VDD voltage itself must continue to ramp up to the operational voltage value. After the POR sequence has started, AM1U1108 will have a period of time to go through all the steps in the sequence and will be ready and completely operational after the Power-Up sequence is completed.

AM1U1108 is powered down and non-operational when the VDD voltage is between 0.6 V and -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher than the VDD voltage is applied to any other pin (although there is a 0.5 V margin due to forward drop voltage of the ESD protection diodes).

All pins are in HIGH IMPEDANCE state while the Power-Up sequence is taking place, and when the chip is powered down. The last step in the Power-Up sequence releases the IO structures from the HIGH IMPEDANCE state making the device operational. The design programmed into the chip defines the pin configuration of the device when operational. (The voltage on pins can't be higher than the VDD and this rule does apply to when the chip is powered on).

13.2. Power-Up Sequence

The Power-Up sequence of signals shown in Figure 13.1.

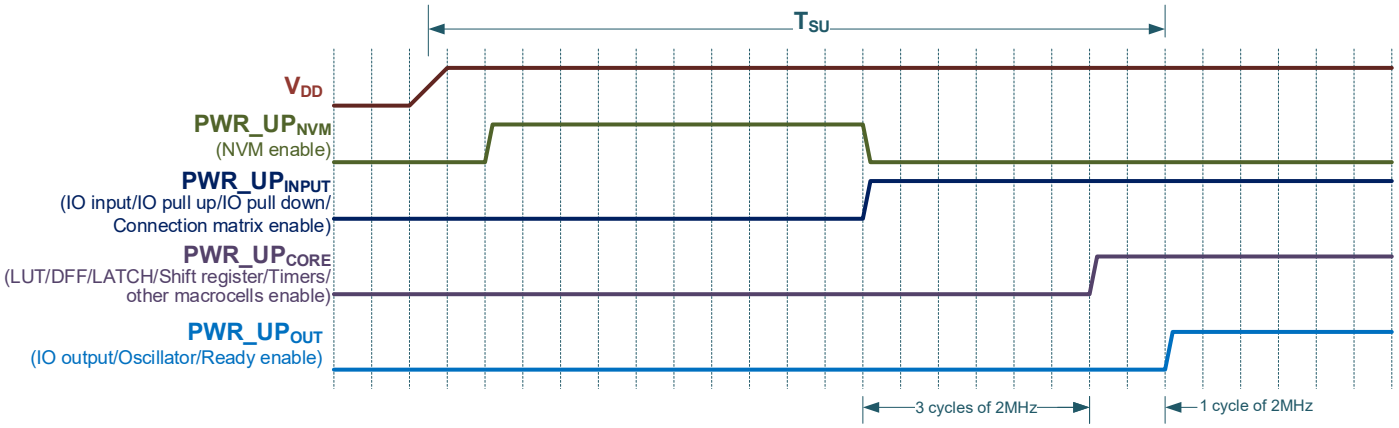


Figure 13.1. POR sequence

As demonstrated by Figure 13.1 after the V_{DD} starts ramping up and crosses the POWER ON threshold, the on-chip NVM memory is enable. After that Input pins and Connection Matrix are enabled and all traces between all macrocells are routed. The macrocells like LUT, DFF, LATCH, Shift Register, Timers and others are initialized and stabilized for the next 3 cycles of 2MHz oscillator. After another one cycle READY signal and OSC outputs are enabled and outputs start run. The output pins, transition from HIGH IMPEDANCE to active at this point.

The completion time for the POR sequence varies by device type in the µASIC family. The completion time also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature to a degree that the times will even vary from chip to chip due to process influence.

13.3. Macrocells Output States During Power-Up Sequence

First, all macrocells have their output set to logic LOW, except the output pins which are in HIGH IMPEDANCE state, before the NVM is enabled. Then until the NVM is ready, all macrocell outputs are unpredictable except the IOs. On the next step Input pins determined by external signals, LOGIC 1 is high, LOGIC 0 is low, LUTs and PDLY macrocell configured as edge detector work according to their inputs. All other macrocells are initialized in the next step. Lastly, READY signal, oscillator and the output pins become active as determined by the input signals. (Figure 13.2 describes the macrocell output signal states during the Power-Up sequence).

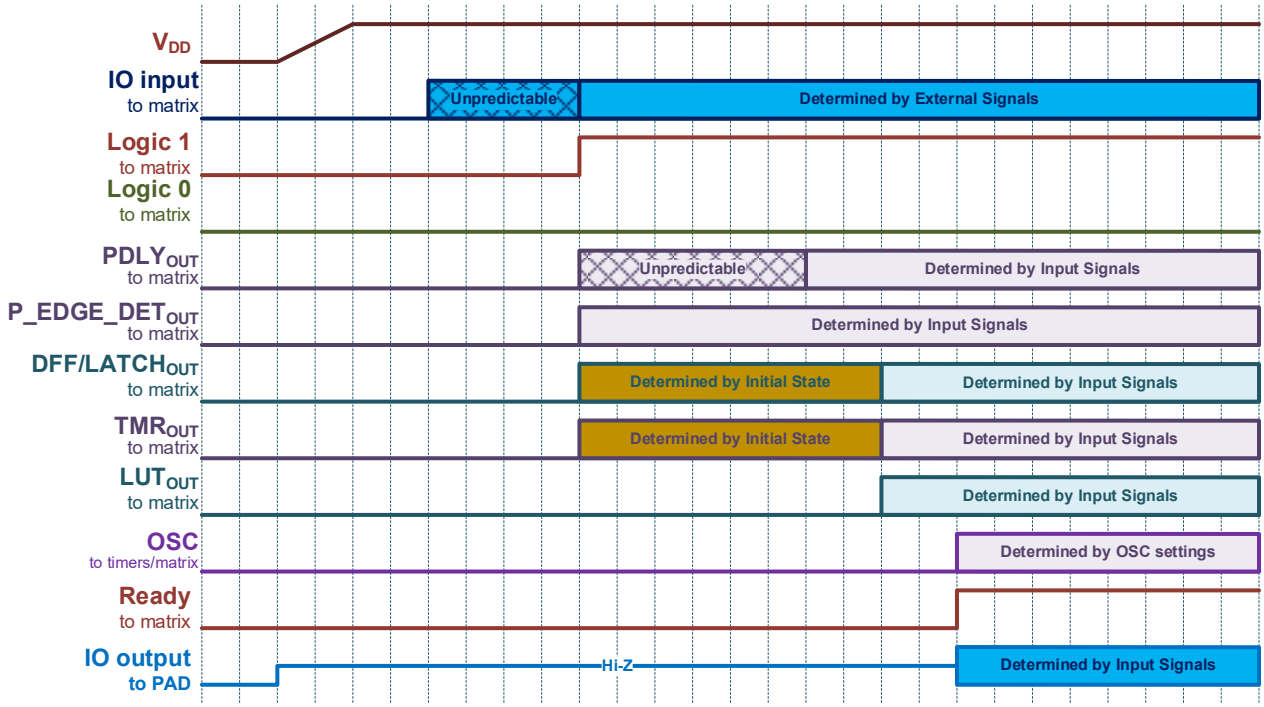


Figure 13.2. Internal Macrocell States during POR sequence

13.4. Reset Events

There are number of reset events for AM1U1108:

- POR;
- CRV;
- IO2 Reset.

CRV (see section 111) and IO2 Reset can be enabled or disabled by register bits (Table 13.1). Keep in mind that IO2 should be configured as Digital IN (any of the input modes) as long as IO2 Reset is enabled.

Table 13.1. IO2 Reset Register Settings

Register Bit Address	Register Name	Register Definition
IO2 Reset		
<499>	IO2_RESET_EN	IO2 Reset: 0: Disable 1: Enable
<498:497>	IO2_RESET_TRIG	IO2 Reset Trigger Event: 00: Rising Edge 01: Falling Edge 10: High Level 11: Reserved

14. Abbreviations

ADJ	Adjustable
ASIC	Application-Specific Integrated Circuit
CLK	Clock
CLK/L	Clock/Latch
CRV	Continuous Registers Verification
CM	Connection Matrix
CMI	Connection Matrix Inputs
CMO	Connection Matrix Outputs
CV	Counted Value
D	Data
DC	Direct Current
DFF	D Flip-Flop
DI	Digital Input
DIR	Direction
DILV	Digital Input Low Voltage
DIO	Digital Input/Output
ED	Edge Detector
ESD	Electrostatic Discharge
EXTCLK	External Clock
GND	Ground
IC	Integrated Circuit
IMC	Input Mode Control
IN	Input
IO	Input/Output
Logic 0	Low Logic Level
Logic 1	High Logic Level
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage
MF	Multi-Functional
MSB	Most Significant Bit
MUX	Multiplexer
N/A	Not Applicable
N/C	Not Connected
NMOS	N channel Metal Oxide Semiconductor
NVM	Non-Volatile Memory
OD	Open Drain
OSC	Oscillator
OSG	One Shot Generator
OUT	Output
PDLY	Programmable Delay
PMOS	P channel Metal Oxide Semiconductor
POR	Power On Reset
PP	Push Pull
PROP	Propagation
PW	Pulse Width
PWRDWN	Power Down
REG	Register
RST	Reset
SHR	Shift Register
ST	Schmitt Trigger
TMR	Timer
TQFN	Thin Quad Flat No Leads
VDD	Voltage Drain-Drain
VSS	Voltage Source-Source
w/	With
w/o	Without

15. Appendix A – AM1U1108 Register Definition

Register Bit Address	Register Name	Register Definition
Connection matrix outputs		
<4:0>	CMO0_IO3_DIN	IO3 DIN
<9:5>	CMO1_IO4_DIN	IO4 DIN
<14:10>	CMO2_IO4_DIR	IO4 DIR
<15>	CRV_B0	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<20:16>	CMO3_MF0_2BLUT0_DFF0_IN0_CLK	MF0(2-bit LUT0/DFF0/LATCH0) IN0/CLK/nL
<25:21>	CMO4_MF0_2BLUT0_DFF0_IN1_D	MF0(2-bit LUT0/DFF0/LATCH0) IN1/D
<30:26>	CMO5_MF1_2BLUT1_DFF1_IN0_CLK	MF1(2-bit LUT1/DFF1/LATCH1) IN0/CLK/nL
<35:31>	CMO6_MF1_2BLUT1_DFF1_IN1_D	MF1(2-bit LUT1/DFF1LATCH1) IN1/D
<40:36>	CMO7_2BLUT2_IN0	2-bit LUT2 IN0
<41>	CRV_B1	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
<42>	CRV_B2	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<43>	CRV_B3	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<48:44>	CMO8_2BLUT2_IN1	2-bit LUT2 IN1
<53:49>	CMO9_2BLUT3_IN0	2-bit LUT3 IN0
<58:54>	CMO10_2BLUT3_IN1	2-bit LUT3 IN1
<63:59>	CMO11_MF2_3BLUT0_DFF2_IN0_CLK	MF2(3-bit LUT0/DFF2/LATCH2) IN0/CLK/nL
<68:64>	CMO12_MF2_3BLUT0_DFF2_IN1_D	MF2(3-bit LUT0/DFF2/LATCH2) IN1/D
<73:69>	CMO13_MF2_3BLUT0_DFF2_IN2_NRST	MF2(3-bit LUT0/DFF2/LATCH2) IN2/nRST
<78:74>	CMO14_MF3_3BLUT1_DFF3_IN0_CLK	MF3(3-bit LUT1/DFF3/LATCH3) IN0/CLK/nL
<83:79>	CMO15_MF3_3BLUT1_DFF3_IN1_D	MF3(3-bit LUT1/DFF3/LATCH3) IN1/D
<84>	CRV_B4	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
<89:85>	CMO16_MF3_3BLUT1_DFF3_IN2_NRST	MF3(3-bit LUT1/DFF3/LATCH3) IN2/nRST
<94:90>	CMO17_MF4_3BLUT2_DFF4_IN0_CLK	MF4(3-bit LUT2/DFF4/LATCH4) IN0/CLK/nL
<99:95>	CMO18_MF4_3BLUT2_DFF4_IN1_D	MF4(3-bit LUT2/DFF4/LATCH4) IN1/D
<104:100>	CMO19_MF4_3BLUT2_DFF4_IN2_NRST	MF4(3-bit LUT2/DFF4/LATCH4) IN2/nRST
<109:105>	CMO20_MF5_3BLUT3_DFF5_IN0_CLK	MF5(3-bit LUT3/DFF5/LATCH5) IN0/CLK/nL
<114:110>	CMO21_MF5_3BLUT3_DFF5_IN1_D	MF5(3-bit LUT3/DFF5/LATCH5) IN1/D
<119:115>	CMO22_MF5_3BLUT3_DFF5_IN2_NRST	MF5(3-bit LUT3/DFF5/LATCH5) IN2/nRST
<124:120>	CMO23_MF6_3BLUT4_SH_REG_IN0_D	MF6(3-bit LUT4/Shift Register) IN0/D
<129:125>	CMO24_MF6_3BLUT4_SH_REG_IN1_NRST	MF6(3-bit LUT4/Shift Register) IN1/nRST
<134:130>	CMO25_MF6_3BLUT4_SH_REG_IN2_CLK	MF6(3-bit LUT4/Shift Register) IN2/CLK
<139:135>	CMO26_MF8_4BLUT0_16BTMR2_IN0_CLK	MF8(4-bit LUT0/16-bit TMR2) IN0/CLK
<140>	CRV_B5	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
<145:141>	CMO27_MF8_4BLUT0_16BTMR2_IN1_RST	MF8(4-bit LUT0/16-bit TMR2) IN1/RST
<150:146>	CMO28_MF8_4BLUT0_16BTMR2_IN2_KEEP	MF8(4-bit LUT0/16-bit TMR2) IN2/KEEP
<155:151>	CMO29_MF8_4BLUT0_16BTMR2_IN3_UP	MF8(4-bit LUT0/16-bit TMR2) IN3/UP
<160:156>	CMO30_8BTMR0_IN_RST	8-bit TMR0 IN/RST
<165:161>	CMO31_8BTMR1_IN_RST	8-bit TMR1 IN/RST
<170:166>	CMO32_8BTMR0_8BTMR1_CLK	8-bit TMR0/8-bit TMR1 CLK
<175:171>	CMO33_8BTMR3_IN_CLK	8-bit TMR3 IN/CLK
<180:176>	CMO34_MF7_PDLY_ED_IN	MF7(PDLY/Edge Detector) IN
<185:181>	CMO35_OSC_PWR_DWN	OSC PWR DWN
<190:186>	CMO36_IO6_DIN	IO6 DIN

Register Bit Address	Register Name	Register Definition
<191>	CRV_B6	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
<196:192>	CMO37_IO7_DIN	IO7 DIN
<201:197>	CMO38_IO8_DIN	IO8 DIN
<206:202>	CMO39_IO8_DIR	IO8 DIR
Reserved		
<214:207>		Reserved
MF0 (2-bit LUT0/DFF0/LATCH0)		
<215>	MF0_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<216>	MF0_LUT_CTRL_DATA_1	1st bit of LUT control data: 0: LOW 1: HIGH
<217>	MF0_LUT_CTRL_DATA_2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<218>	MF0_LUT_CTRL_DATA_3	3rd bit of LUT control data: 0: LOW 1: HIGH
CRV		
<219>	CRV_B7	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
MF1 (2-bit LUT1/DFF1/LATCH1)		
<220>	MF1_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<221>	MF1_LUT_CTRL_DATA_1	1st bit of LUT control data: 0: LOW 1: HIGH
<222>	MF1_LUT_CTRL_DATA_2_DFF_LATCH_INIT_STATE	2nd bit of LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<223>	MF1_LUT_CTRL_DATA_3	3rd bit of LUT control data: 0: LOW 1: HIGH
OSC		
<225:224>	OSC_FREQ_SEL	Frequency: 00: Both disable 01: 25kHz 10: 2MHz 11: Both enable
<226>		Reserved
2-bit LUT2		
<230:227>	2BLUT2_CTRL_DATA	OUT LUT control data

Register Bit Address	Register Name	Register Definition
2-bit LUT3		
<234:231>	2BLUT3_CTRL_DATA	OUT LUT control data
Multifunctional macrocells		
<235>	MF0_MODE	MF mode: 0: LUT 1: DFF/LATCH
<236>	MF1_MODE	MF mode: 0: LUT 1: DFF/LATCH
MF2 (3-bit LUT0/DFF2/LATCH2)		
<237>	MF2_LUT_CTRL_DATA0_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<238>	MF2_LUT_CTRL_DATA0_1	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH
<239>	MF2_LUT_CTRL_DATA0_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<240>	MF2_LUT_CTRL_DATA0_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<241>	MF2_LUT_CTRL_DATA0_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<242>	MF2_LUT_CTRL_DATA0_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<243>	MF2_LUT_CTRL_DATA0_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<244>	MF2_LUT_CTRL_DATA0_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<252:245>	MF2_LUT_CTRL_DATA1	OUT1 LUT control data
MF3 (3-bit LUT1/DFF3/LATCH3)		
<253>	MF3_LUT_CTRL_DATA0_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<254>	MF3_LUT_CTRL_DATA0_1	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH
<255>	MF3_LUT_CTRL_DATA0_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET

Register Bit Address	Register Name	Register Definition
<256>	MF3_LUT_CTRL_DATA0_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<257>	MF3_LUT_CTRL_DATA0_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<258>	MF3_LUT_CTRL_DATA0_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<259>	MF3_LUT_CTRL_DATA0_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<260>	MF3_LUT_CTRL_DATA0_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<268:261>	MF3_LUT_CTRL_DATA1	OUT1 LUT control data
MF4 (3-bit LUT2/DFF4/LATCH4)		
<269>	MF4_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH
<270>	MF4_LUT_CTRL_DATA_1_Q_POL	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<271>	MF4_LUT_CTRL_DATA_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<272>	MF4_LUT_CTRL_DATA_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<273>	MF4_LUT_CTRL_DATA_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<274>	MF4_LUT_CTRL_DATA_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<275>	MF4_LUT_CTRL_DATA_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<276>	MF4_LUT_CTRL_DATA_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH
MF5 (3-bit LUT3/DFF5/LATCH5)		
<277>	MF5_LUT_CTRL_DATA_0_DFF_LATCH_SEL	0th bit of OUT0 LUT control data: 0: LOW 1: HIGH or DFF/LATCH selection: 0: DFF 1: LATCH

Register Bit Address	Register Name	Register Definition
<278>	MF5_LUT_CTRL_DATA_1_Q_POL	1st bit of OUT0 LUT control data: 0: LOW 1: HIGH or Q polarity of DFF/LATCH: 0: Q 1: nQ
<279>	MF5_LUT_CTRL_DATA_2_DFF_LATCH_NRST_NSET_SEL	2nd bit of OUT0 LUT control data: 0: LOW 1: HIGH or nRESET/nSET selection: 0: nRST 1: nSET
<280>	MF5_LUT_CTRL_DATA_3_DFF_LATCH_INIT_STATE	3rd bit of OUT0 LUT control data: 0: LOW 1: HIGH or Initial state of DFF/LATCH: 0: LOW 1: HIGH
<281>	MF5_LUT_CTRL_DATA_4	4th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<282>	MF5_LUT_CTRL_DATA_5	5th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<283>	MF5_LUT_CTRL_DATA_6	6th bit of OUT0 LUT control data: 0: LOW 1: HIGH
<284>	MF5_LUT_CTRL_DATA_7	7th bit of OUT0 LUT control data: 0: LOW 1: HIGH
MF6 (3-bit LUT4 / Shift register)		
<288:285>	MF6_LUT_CTRL_DATA3_0_SHIFT_REG_STAGE_OUT0	Low tetrad of OUT LUT control data or stage of OUT0 shift register
<292:289>	MF6_LUT_CTRL_DATA7_4_SHIFT_REG_STAGE_OUT1	High tetrad of OUT LUT control data or stage of OUT1 shift register
Multifunctional macrocells		
<293>	MF2_MODE	MF mode: 0: LUT 1: DFF/LATCH
<294>	MF3_MODE	MF mode: 0: LUT 1: DFF/LATCH
<295>	MF4_MODE	MF mode: 0: LUT 1: DFF/LATCH
<296>	MF5_MODE	MF mode: 0: LUT 1: DFF/LATCH
MF6 (3-bit LUT4 / Shift register)		
<297>	MF6_MODE	MF mode: 0: LUT 1: Shift register
<298>	MF6_SHIFT_REG_OUT1_POL	Shift register OUT1 polarity: 0: OUT1 1: nOUT1
MF8 4-bit LUT0/16-bit TMR2)		
<314:299>	MF8_CTRL_DATA	MF control data
<316:315>	MF8_TMR_MODE	Timer mode: 00: Delay 01: One shot 10: Frequency detector 11: Counter

Register Bit Address	Register Name	Register Definition
<319:317>	MF8_TMR_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR1_OUT
<321:320>	MF8_TMR_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<322>	MF8_TMR_RST_FUNC	Reset functionality: 0: Reset to 0 1: Set to Control data
<323>	MF8_TMR_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<324>	MF8_MODE	MF mode: 0: LUT 1: Timer
OSC		
<325>	OSC_PWR_MODE	Power mode: 0: Auto power on 1: Forced power on
<326>	OSC_PWR_ON_TIME	Power on time: 0: Normal 1: Fast
<327>	CRV_B8	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
<329:328>	OSC_PRESCALER_MAIN	Main prescaler: 00: 1 01: 1/2 10: 1/4 11: 1/8
<332:330>	OSC_PRESCALER_OUT0	OUT0 prescaler: 000: OUT0_DISABLE 001: OSC_CLK 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<335:333>	OSC_PRESCALER_OUT1	OUT1 prescaler: 000: OUT1_DISABLE 001: OSC_CLK/2 010: OSC_CLK/4 011: OSC_CLK/8 100: OSC_CLK/16 101: OSC_CLK/32 110: OSC_CLK/64 111: OSC_CLK/128
<336>	OSC_CLK_SOURCE_SEL	Clock source: 0: Inner oscillator 1: External CLK
IOs		
<337>	IO3_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2

Register Bit Address	Register Name	Register Definition
<338>	IO4_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<339>	IO6_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
<340>	IO7_DRIVE_STRENGTH	Drive strength: 0: ×1 1: ×2
CRV		
<342>	CRV_B9	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
8-bit TMR0		
<350:343>	TMR0_CTRL_DATA	Timer control data
<352:351>	TMR0_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<355:353>	TMR0_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR3_OUT
<358:356>	TMR0_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<359>	TMR0_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
8-bit TMR1		
<367:360>	TMR1_CTRL_DATA	Timer control data
CRV		
<368>	CRV_B10	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
IOs		
<369>	IO3_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<370>	IO4_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<371>	IO6_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<372>	IO7_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)
<373>	IO8_FORCE_IN_EN	Force input: 0: Disable 1: Enable (Input is always ON)

Register Bit Address	Register Name	Register Definition
OSC		
<374>	OSC_OUT0_EN	OUT0 enable: 0: OUT0 disable 1: OUT0 enable
<375>	OSC_OUT1_EN	OUT1 enable: 0: OUT1 disable 1: OUT1 enable
CRV		
<376>	CRV_B11	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
<377>	CRV_B12	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
8-bit TMR1		
<379:378>	TMR1_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: High level reset (counter)
<382:380>	TMR1_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR0_OUT
<385:383>	TMR1_MODE	Timer mode: 000: Delay 001: One shot 010: Frequency detector 011: Counter 100: Edge detector 101: Delayed edge detector 110: Reserved 111: Reserved
<386>	TMR1_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
<387>		Reserved
8-bit TMR3		
<395:388>	TMR3_CTRL_DATA	Timer control data
<397:396>	TMR3_MODE	Timer mode: 00: Delay 01: One shot 10: Frequency detector 11: Counter
<400:398>	TMR3_CLK	CLK source: 000: OSC 001: OSC/4 010: OSC/8 011: OSC/16 100: OSC/64 101: OSC/128 110: External CLK 111: TMR0_OUT
<402:401>	TMR3_TRIG_EVENT	Timer trigger event: 00: On both falling and rising edges 01: On falling edge only 10: On rising edge only 11: Reserved

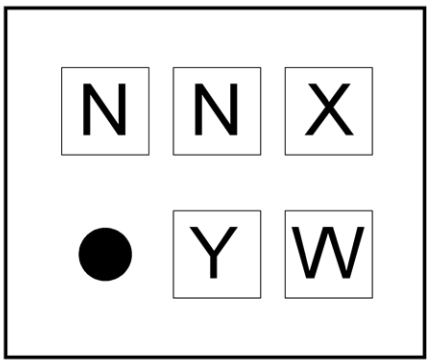
Register Bit Address	Register Name	Register Definition
<403>	TMR3_OUT_POL	Polarity of timer output: 0: OUT 1: nOUT
IOs		
<404>	IO3_DIR	Direction: 0: Input 1: Output
<405>	IO6_DIR	Direction: 0: Input 1: Output
IO2		
<408:407>	IO2_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<410:409>	IO2_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
CRV		
<411>	CRV_B13	CRV bit. If CRV is enabled, please make sure to keep the bit HIGH
IO3		
<413:412>	IO3_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<415:414>	IO3_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<417:416>	IO3_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<418>	IO3_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
IO4		
<420:419>	IO4_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<422:421>	IO4_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<424:423>	IO4_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<425>	IO4_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up

Register Bit Address	Register Name	Register Definition
IO6		
<427:426>	IO6_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<429:428>	IO6_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<431:430>	IO6_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<432>	IO6_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
IO7		
<434:433>	IO7_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<436:435>	IO7_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<438:437>	IO7_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<439>	IO7_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
IO8		
<441:440>	IO8_IMC	Input mode control: 00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Digital Input Low Voltage 11: Reserved
<443:442>	IO8_OMC	Output mode control: 00: Push Pull 01: Open Drain NMOS 10: Open Drain PMOS 11: Reserved
<445:444>	IO8_PULL_R_VAL	Pulled resistor value: 00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
<446>	IO8_PULL_R_DOWN_UP_SEL	Pull resistor: 0: Down 1: Up
System		
<454:447>	SYS_PATTERN_ID	Project pattern ID
<455>		Reserved
Security control		
<456>	SYS_SECURITY_CRV_EN	Continuous register verification: 0: Disable 1: Enable
<457>		Reserved

Register Bit Address	Register Name	Register Definition
MF7 (PDLY/Edge Detector)		
<458>	MF7_OUT_POL	Output polarity: 0: OUT 1: nOUT
<460:459>	MF7_MODE	MF mode: 00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
<462:461>	MF7_DELAY_VAL	Delay value: 00: 140ns 01: 280ns 10: 420ns 11: 560ns
TMRs		
<470:463>		Reserved
<472:471>	TMR0_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<474:473>	TMR1_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<486:475>		Reserved
<488:487>	MF8_TMR_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
<494:489>		Reserved
<496:495>	TMR3_INIT_STATE	Timer initial state: 00: Initial 0 01: Initial 1 10: Bypass initial 11: Bypass initial
IO2 reset		
<498:497>	IO2_RESET_TRIG	IO2 Reset Trigger Event: 00: Rising Edge 01: Falling Edge 10: High Level 11: Reserved
<499>	IO2_RESET_EN	IO2 Reset: 0: Disable 1: Enable
<500>		Reserved
CRV		
<501>	CRV_B14	CRV bit. If CRV is enabled, please make sure to keep the bit LOW
Reserved		
<511:502>		Reserved

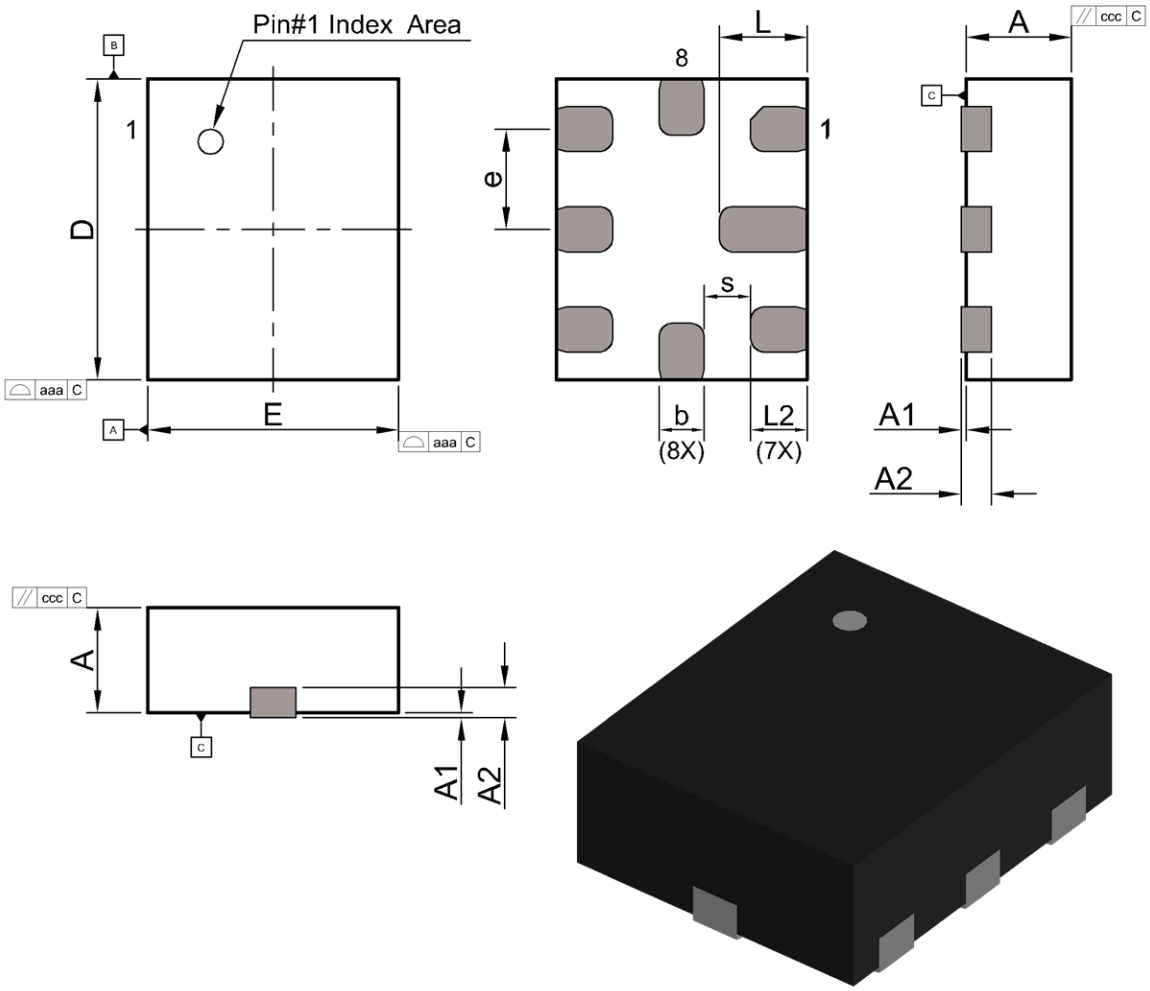
16. Package Top Marking System Definition

(Top View)



NN - Identification Code
X - Internal Code
Y - Assembly Year
W - Assembly Week

17. Package Drawing and Dimensions



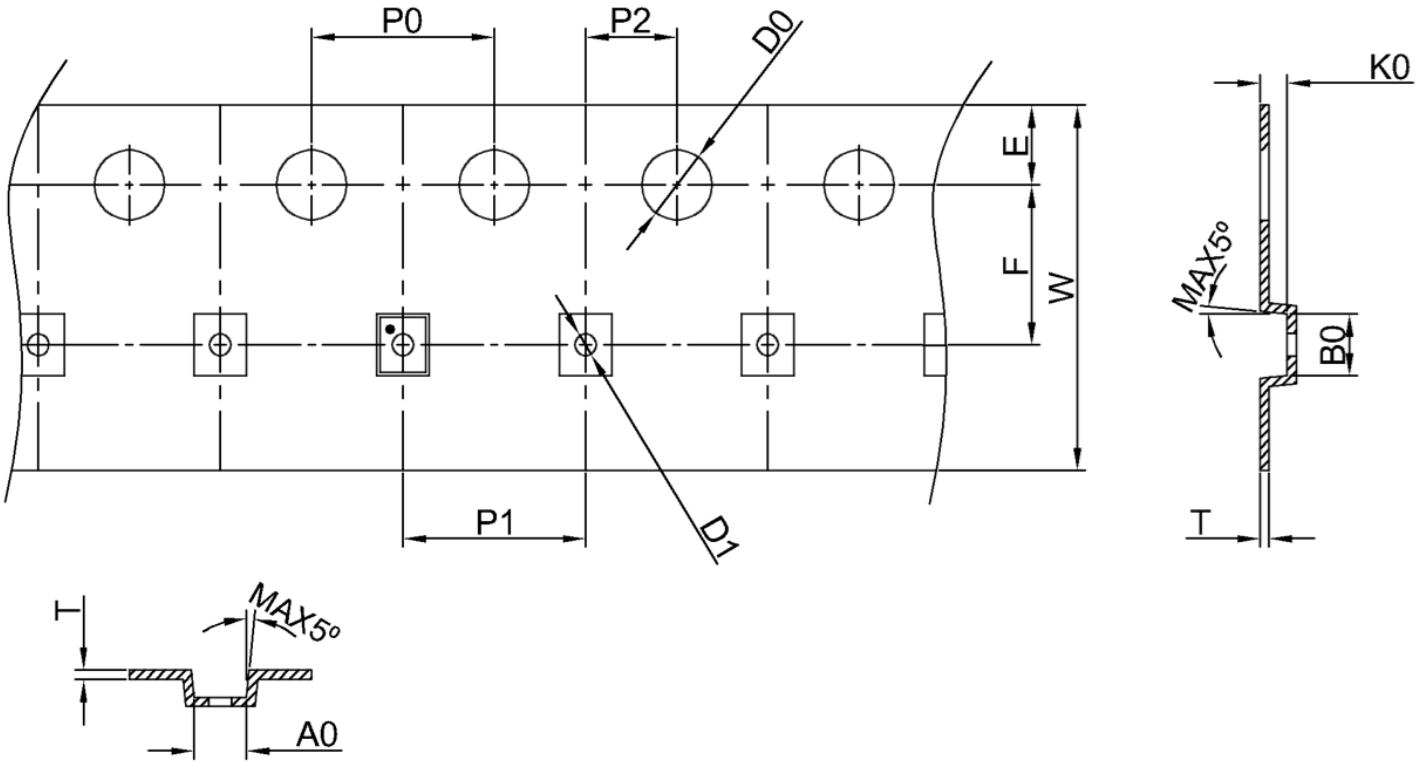
TQFN-8							
Dim	**Min**	**Max**	**Typ**	**Dim**	**Min**	**Max**	**Typ**
A	0.37	0.47	0.42	**e**	--	--	0.40
A1	-0.005	0.03	--	**L**	--	--	0.35
A2	0.10	0.15	0.12	**L2**	--	--	0.225
b	--	--	0.18	**s**	--	--	0.185
D	1.15	1.25	1.20	**aaa**	--	--	0.05
E	0.95	1.05	1.00	**ccc**	--	--	0.05
All Dimensions in mm							

18. Tape and Reel Specifications

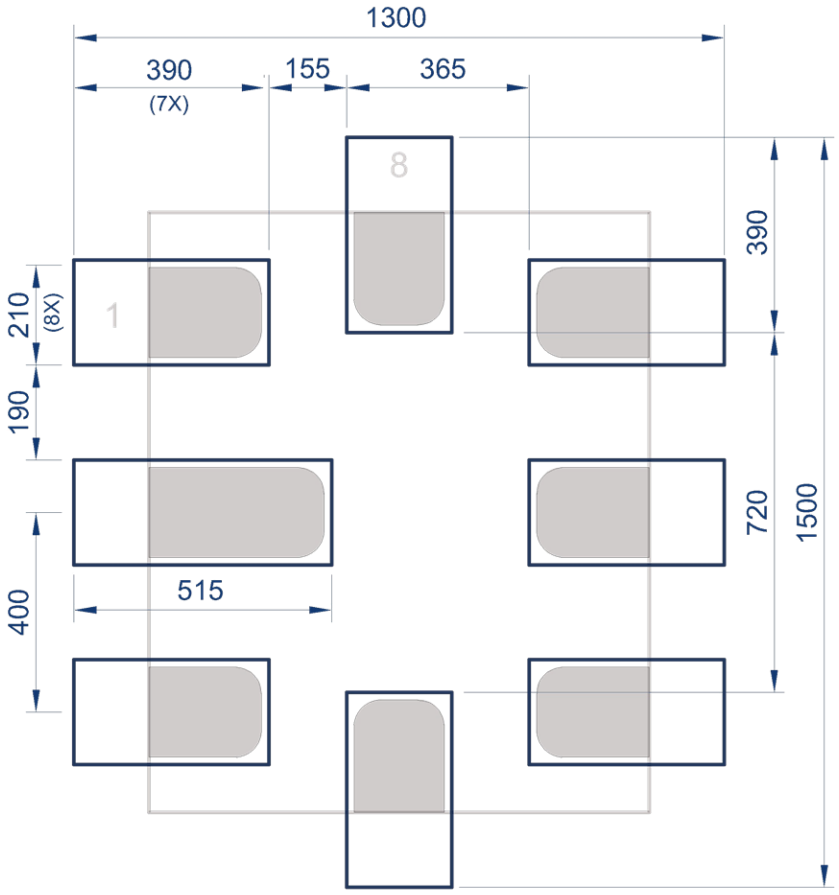
Package Type	# of Pins	Nominal Package Size, mm	Max Units		per Reel & Hub Size, mm	Leader (min)		Trailer (min)		Tape Width, mm	Part Pitch, mm
			per Reel	per Box		Pockets	Len gth, mm	Pockets	Length, mm		
TQFN 8L 0.4P FC	8	1.0× 1.2× 0.42	3000	3000	178/55	130	520	130	520	8	4

18.1. Carrier Tape Drawing and Dimensions

Package Type	A0	B0	K0	P0	P1	P2	T	E	F	D0	D1	W
X1-QFN1012-8 (Type AX)	1.15	1.35	0.60	4.00	4.00	2.00	0.20	1.75	3.50	1.55	0.50	8.00



19. Recommended Land Pattern



Unit: um

20. Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Weight: 0.0014 grams (Approximate)

21. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.504 mm^3 (nominal). More information can be found at www.jedec.org.

22. Revision History

Date	Version	Change
February 02, 2022	Rev.001	Initial release.
July 12, 2022	Rev.002	Section Macrocell function summary updated with Macrocell Manifest at the beginning of the datasheet.
September 07, 2022	Rev.003	Updated IO structure diagrams
April 06, 2023	Rev.004	Updated section 4. Electrical Specifications
September 12, 2023	Rev.005	Updated Section 4. Electrical Specifications. Completed section 22. Worldwide Sales and Customer Support. Updated section 12. Oscillator (OSC).
January 26, 2024	Rev.006	Updated diagrams and figures. Fixed typos. Added initial states for timers: TMR0_INIT_STATE, TMR1_INIT_STATE, MF8_TMR_INIT_STATE, and TMR3_INIT_STATE.
September 26, 2024	Rev.007	Updated the section 16. Package Top Marking System Definition. Updated oscillator settling time definition. Updated Electrical Specifications. Fixed typos.
September 23, 2025	Rev.008	Updated electrical specifications. Updated Figure 13.1. POR sequence. Added a section Mechanical Data. Updated the section Data Protection. Updated Package Dimensions.
March 3, 2026	Rev.009	Updated Tape and Reel Specification. Updated section 4. Electrical Specifications: IO high-level input voltage V_{IH} for digital input low voltage mode; HIGH-Level Output Current I_{OH} for Push-Pull ×2, and Opdan Drain PMOS ×2.

23. Worldwide Sales and Customer Support

Atlas Magnetics has established a vast network of offices, partners, distributors, and manufacturer's representatives. Feel free to contact any of the listed contacts to get in touch with us.

WEB support:
atlasmagnetics.com/contact

AM direct contacts:

Americas:
alexr@atlasmagnetics.com

Taiwan, China, South Eastern Asia:
ycchang@atlasmagnetics.com

EMEA:
Dmytro.Ulianov@atlasmagnetics.com

Distributors:

EMEA:

EPS Global

epsglobal.com
atlas@epsglobal.com

DUBLIN, IRELAND (HQ)
Unit 17 Kinsealy Business Park,
Kinsealy, Co. Dublin
Ireland
Phone: +353 1 8038918

DARMSTADT, GERMANY
Rheinstrasse 41, 64283
Darmstadt, Germany
Phone: +49 6151 501 2454

BRNO, CZECH REPUBLIC
Electronic Product Services
Czech, s.r.o.
Technology Park, Building B2
Podnikatelská 2902/4
612 00 Brno, Czech Republic
Phone: +420 541 215 126

TIMISOARA, ROMANIA
Calea Torontalului DN 6, km 6,
PITT parcela C1 Timisoara
Timisoara, Romania
Phone: +40 256 22 33 07

READING, UNITED KINGDOM
14A Church Street, aversham
Reading, RG4 8AU
United Kingdom
Phone: +44 (0)20 3008 9709

WARSAW, POLAND
Ul. Polna 48/31
00-644, Warszawa
Poland
Phone: +48 22 825 10 92

Taiwan, China, Southeast Asia:

Alltek

alltek.com
yvonnetsai@alltek.com

Taipei, Taiwan
9F, No.360, Ruei Guang Rd., Neihu, Taipei, Taiwan 114, R.O.C.
E-mail: yvonnetsai@alltek.com
Phone: +886 226275859 # 141

Sales representatives:

Cedar Technologies

cedartech.co.uk
info@cedartech.co.uk

United Kingdom:
Paul Richardson
Email: paul@cedartech.co.uk
Tel: +44 7747 865040
Sean Lynch
Email: sean@cedartech.co.uk
Tel: +44 7775 923518

Sweden:
Michel Olsson
Email: Michel@cedartech.se
Tel: +46 70 026 2330
Bo Molander
Email: Bo@cedartech.se
Tel: +46 73 708 3570

Finland and Baltics:
Mika Rakkolainen
Email: mika@cedartech.co.uk
Tel: +358 503308400

Norway:
Brian Märcher
Email: brian@cedartech.dk
Tel: +45 30527018

Poland:
Piotr Wloczewski
Email: piotr@cedartech.pl
Tel: +48 605 308 216

Denmark:
Morten Møller
Email: morten@cedartech.dk
Tel: +45 53600898

Westmark Electronics

westmarkco.com
sales@westmarkco.com

Washington Office - HQ:
1750 - 112th Avenue NE Suite
C225 Bellevue, WA 98004
Phone: 425-454-1944
Territories: Washington,
Northern Idaho, Alaska,
Montana

Oregon Office:
8705 SW Nimbus Ave., Suite
320 Beaverton, OR 97008
Phone (503) 641-8780
Territories: Oregon, Southern
Idaho, SW Washington
(Vancouver, WA)

British Columbia Office:
5-7488 Mulberry Place
Burnaby, BC Canada V3N 5B4
Phone: (778) 929-2858
Territories: British Columbia,
Alberta, Manitoba, &
Saskatchewan

MRB

mrbsales.net
info@mrbsales.net

MRB Sales, Inc.
16801 Addison Road Suite 375, Addison, Texas 75001
972-250-2900 (Main)
972-250-2905 (FAX)
Territories: Texas, Oklahoma, Louisiana, Arkansas, Kansas, Country of Mexico

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